FABRICATION TECHNIQUES FOR MICRO-OPTICAL DEVICE ARRAYS

THESIS

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Abstract
Micro-optical devices are vital components of conventional military data storage, sensor, and communication systems. Two types of micro-optical device arrays exist: individually addressable and matrix addressable. The matrix addressable array has a drastically reduced number of metal lines and can potentially be fabricated into large, dense (over 1k elements) arrays. Such arrays are expected to enable the development of extremely high bandwidth optical interconnect systems for future military applications including optical computing and short-haul fiber optical communication systems. I investigate new fabrication techniques for the assembly of dense matrix-addressed arrays of micro-optical devices such as vertical-cavity surface-emitting lasers. Using a micro-electro-mechanical systems (MEMS) foundry process, I design a test chip that consists of a variety of array configurations to explore possible assembly techniques. I also design a new photolithographic mask set based on assembly by flip-chip bonding and fluidic self-assembly techniques. Using my mask set, I perform basic fabrication studies and an analysis of metallization schemes for the realization of dense emitter and detector arrays. Finally, I develop and characterize three methods for array fabrication including a novel substrate trenching technique and involving the use of a spin-on polymer (poly-methyl-glutarimide or PMGI) that serves as an insulating and planarization layer between row and column metal lines.

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FABRICATION TECHNIQUES FOR MICRO-OPTICAL DEVICE ARRAYS

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Abstract

Micro-optical devices are vital components of conventional military data storage, sensor, and communication systems. Two types of micro-optical device arrays exist: individually addressable and matrix addressable. The matrix addressable array has a drastically reduced number of metal lines and can potentially be fabricated into large, dense (over 1k elements) arrays. Such arrays are expected to enable the development of extremely high bandwidth optical interconnect systems for future military applications including optical computing and short-haul fiber optical communication systems.

I investigate new fabrication techniques for the assembly of dense matrix-addressed arrays of micro-optical devices such as vertical-cavity surface-emitting lasers. Using a micro-electro-mechanical systems (MEMS) foundry process, I design a test chip that consists of a variety of array configurations to explore possible assembly techniques. I also design a new photolithographic mask set based on assembly by flip-chip bonding and fluidic self-assembly techniques. Using my mask set, I perform basic fabrication studies and an analysis of metallization schemes for the realization of dense emitter and detector arrays. Finally, I develop and characterize three methods for array fabrication including a novel substrate trenching technique and involving the use of a spin-on polymer (poly-methyl-glutarimide or PMGI) that serves as an insulating and planarization layer between row and column metal lines.

FABRICATION TECHNIQUES FOR MICRO-OPTICAL DEVICE ARRAYS

1. Introduction

1.1 Background

Since their development in the early 1960's, semiconductor lasers have made significant contributions in many optical areas involving communications, data storage, and sensors. Edge-emitting lasers, the first to be commercialized and most common semiconductor laser in use today, can be found in bar code scanners, laser pointers, advanced optical memories (CD-ROMs), digital video disk (DVD) players, printers, and multi-channel optical fiber communications [1]. With the recent development of oxide apertures that significantly lower the threshold current and increase the power efficiency, vertical-cavity surface-emitting lasers (VCSELs) have become a more attractive choice for systems that require semiconductor lasers since they offer many advantages over edge-emitting lasers. VCSELs are less expensive, smaller, and easier to fabricate then edge-emitting lasers. In addition, dense two-dimensional VCSEL arrays, as well as arrays of resonant cavity light emitting diodes (RCLEDs) and resonant cavity photodetectors (RCPDs), can be fabricated on a single wafer. One-dimensional edge-emitting laser arrays are readily fabricated, but two-dimensional edge-emitting laser arrays require extensive processing and assembly.

In fabricating micro-optical device arrays, the limiting factor on the size of the array is not the actual devices themselves, but the metal connections required to activate the devices. Micro-optical devices operate by placing a current across the device. To induce the current flow, two

metal connections must be placed on the device, a bottom and top contact. In individually addressable arrays, each device must have at least one of its own metal lines. However, for matrix addressable arrays, devices share lines. Therefore, matrix addressable arrays allow for much denser and larger arrays. The drawback with matrix addressable arrays is that some control is lost over which devices can be turned on at a given time.

The ability to integrate micro-optical device arrays with integrated circuits is critical for the development of optoelectronic integrated circuits (OEICs). The main application for OEICs is telecommunications. With wavelength division-multiplexing and dense wavelength division multiplexing, integration has the potential to offer significant performance improvements [2]. A potential application for integrated VCSEL arrays is in relaying information between or within computers. As very large-scale integrated (VLSI) circuits and ultra large scale integrated (ULSI) circuits reach the limitations of silicon technology, alternative foundries must be utilized to continue advancing the performance of today's electronics. Multi-GHz bandwidth optical interconnects from board to board or chip to chip offer an attractive solution to the electrical interconnect problems of signal integrity and cross-talk at high frequencies [4].

Two primary techniques have been developed to fabricate two-dimensional micro-optical device arrays. The first method is to deposit metal on the backside of a doped substrate to provide a common ohmic contact for all of the devices, grow the devices on the wafer, and then provide an individual contact for each device. The other method is to create heavily doped channels on the substrate with devices on them. The channels are electrically isolated from one another. Finally, metal rows are placed across the tops of the devices, perpendicular to the doped channels to enable matrix addressing of devices.

The ability to fabricate large dense arrays using these techniques is hindered either by the number of metal connections required or the resistance of the doped line. Alternative design approaches and innovative fabrication techniques are required to overcome these limitations. One possible solution is to take advantage of the matrix addressing design and use gold lines to reduce the resistance. This solution, however, contains a new set of fabrication and design problems. There are two main concerns that need to be addressed, each with their own problems. The first being that the metal lines need to contact both the top and bottom surface of the device while electrical isolation must be maintained to avoid cross-talk between active lines and inactive lines. Secondly, the devices cannot be grown directly on top of the metal, therefore, the devices must be transferred onto the lines.

1.2 Problem Statement and Scope

The purpose of this thesis is to study and develop fabrication steps that enable matrix addressing of micro-optical devices using metal lines for electrical contacts. Various approaches will be attempted and analyzed to fabricate the matrix array. Fabrication studies will be conducted on the processing of actual microcavity light-emitter devices. Both flip-chip bonding (FCB) and fluidic self-assembly (FSA) processes will be discussed as possible techniques for the integration of the micro-optical devices onto the array.

I performed all of the photolithography, wet etching, and metal lift-off steps in the AFIT cleanroom. Technicians at the Air Force Research Laboratory's Sensors Directorate cleanroom performed the UV exposure. Metal was deposited onto the wafer at both facilities. The microcavity light-emitter composition was grown at the University of New Mexico [3].

1.3 Approach/Methodology

The first thing that I did was to design the prototype photolithography masks that would be needed to fabricate the VCSELs and the matrix-addressable arrays. In addition, a Multi-User MEMS Process (MUMPs®) chip was designed to explore various foundry configurations for the foundation of the array. I then performed studies on the processing of light-emitter devices so that they can be integrated into the array. Finally, I conducted studies to develop fabrication techniques for the matrix addressable array.

1.4 Accomplishments

For this thesis, I performed a numerical analysis of the microcavity light-emitting devices used for this study. I calculated and compared the resistance for a gold line compared to an n^+-doped GaAs line. I designed prototype photomasks necessary for the processing of the matrix addressable array and the devices. I also designed a MUMPs® chip and had it fabricated. I laid down ring contacts for the development of the microcavity light-emitter devices and performed a wet etch study for the mesa formation of the devices. I was also able to develop three potential methods for the fabrication of a low resistance matrix addressed micro-optical device array.

1.5 Thesis Outline

In Chapter 2, I discuss previously published research relevant to this thesis. In Chapter 3, I describe my design approach and mask layouts and present my numerical analysis and resistance calculations. Chapter 4 then outlines essential experimental equipment and procedures. Chapter 5 contains the experimental results and analysis. Finally, Chapter 6 contains my conclusions and recommendations for future work.

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2. Literature Review

2.1 Introduction

In this chapter, I first discuss the operation and structure of the VCSEL. I then present the two types of arrays, the individually addressable and the matrix addressable, that have been previously fabricated and compare the benefits and limitations of each. Fluidic self-assembly, epitaxial lift-off, and flip-chip bonding are discussed as successful integration methods for the transfer of micro-devices from one substrate to another. Selective oxidation and its importance for device lift-off is then presented. A brief overview of MEMS and the MUMPs® process concludes the chapter.

2.2 Vertical Cavity Surface Emitting Lasers (VCSELs)

While this thesis involves micro-optical device array structures, I will focus on the VCSEL. The VCSEL is one of the most ubiquitous micro-optical devices. Its structure and operation are simply more complex versions of the other micro-optical devices. Other micro-optical devices include the resonant cavity light emitting diode (RCLED), which is a VCSEL structure with fewer distributed Bragg reflector (DBR) periods, and the resonant cavity photo detector (RCPD), which is an RCLED that absorbs light rather than emits it.

VCSELs are semiconductor lasers that emit a beam of light perpendicular to their planar surface. VCSELs consist of doped DBR mirror stacks and a microcavity active region. The DBRs function as mirrors for the device and the microcavity is designed to be a resonant cavity by requiring its thickness to be an integer multiple of $\lambda/2$, where λ is the DBR design wavelength. There are two basic types of VCSELs, bottom-emitting and top-emitting [6]. In bottom-emitting VCSELs, the bottom DBR has a lower reflectance than the top DBR and light is

emitted through the substrate. For bottom-emitting VCSELs, the substrate must be transparent at the operating wavelength. In top-emitting VCSELs, the top DBR has fewer layers than the bottom DBR, thereby giving the top DBR a lower reflectance. The metal contact typically has a circular aperture to allow the light out. Figure 1 illustrates example bottom and top-emitting VCSEL structures.

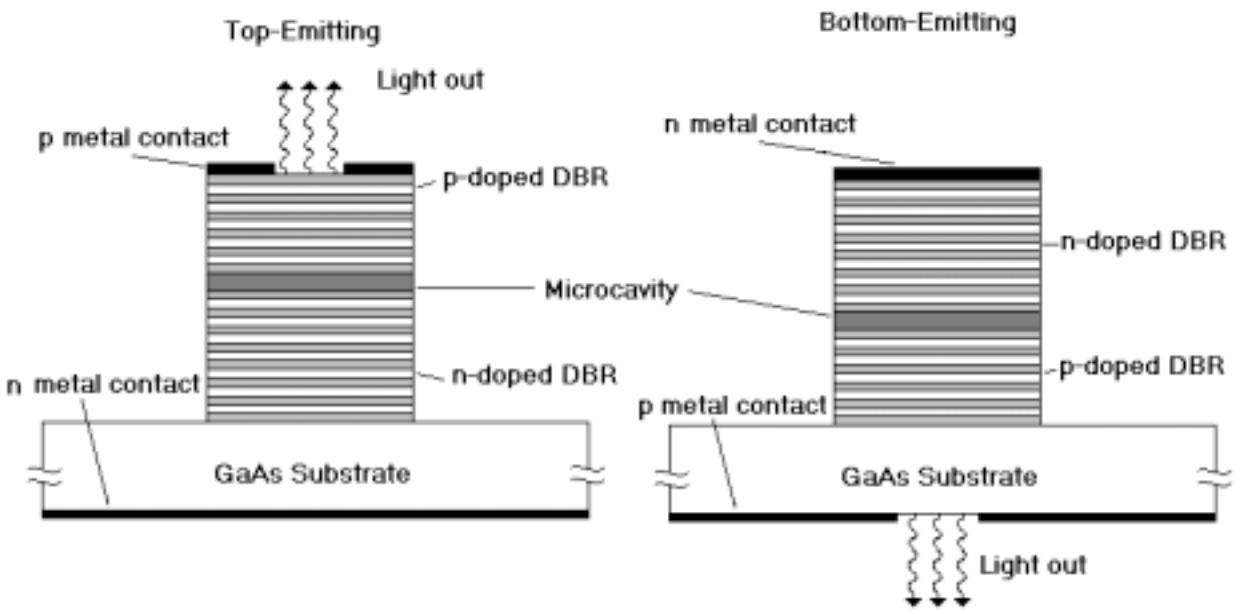

Figure 1 Top and bottom emitting VCSELs.

Light is created in the VCSEL by forward biasing the p-i-n junction that is formed from the doped DBRs and the unintentionally doped microcavity. When a forward bias voltage is applied, the potential difference between the n-doped DBR and the p-doped DBR is reduced. This causes electrons and holes to flow across the device in opposite directions. Once in the microcavity, the electrons and holes are confined in narrow regions called quantum wells, where the energy band gap is small relative to the rest of the structure. Once trapped, the electrons and holes recombine with each other and light energy is released in the form of a photon. Figure 2 illustrates this

process. As the photons reflect off the DBRs and reenter the microcavity, they cause other electron-hole pairs to recombine. This results in the stimulated emission of photons. If more photons are created than are lost in one round trip through the cavity, the VCSEL will begin to lase.

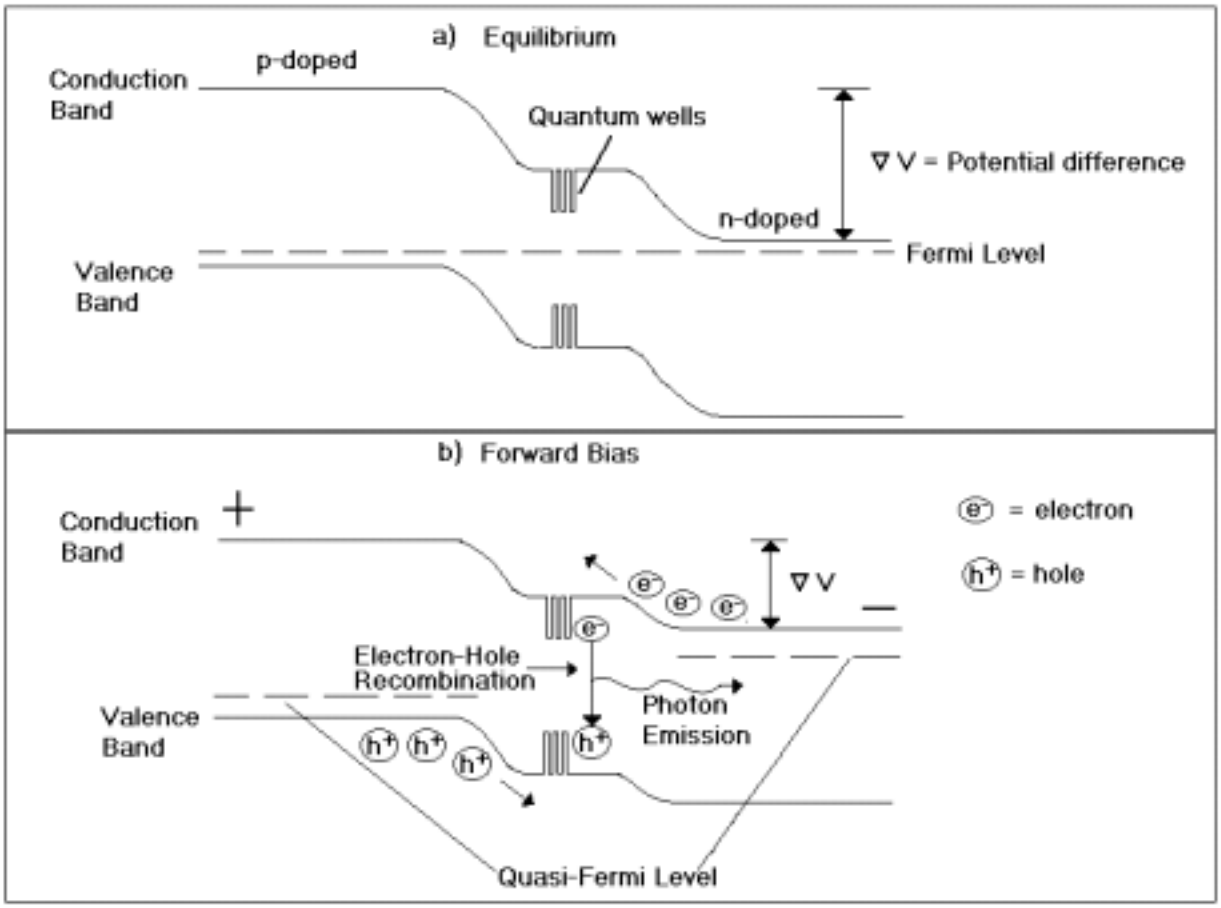

Figure 2 Energy band diagram under a) no bias and b) forward bias.

2.2.1 DBRs

Unlike an edge-emitting laser which has a large gain region with a length of a couple of hundred micrometers, a VCSEL has a total gain region on the order of a few hundred Angstroms. The gain region is the area of the device where photons are created. Consequently, the VCSEL's

mirrors must have a very high reflectivity in order for the optical gain to be greater than the loss [24]. Though metal mirrors are highly reflective, they have absorptive losses. Metal mirrors can only achieve a reflectivity of approximately 98% with the rest of the energy lost in the material by absorption. VCSELs require a DBR reflectance of 99% to 99.99%. To avoid absorption, semiconductor materials are used to make the VCSEL's DBRs. This results in the required high mirror reflectance. The semiconductor material reflects a portion and transmits the remaining energy. The reflectance at the interface of two different nonabsorbing materials at normal incidence is

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2} \right)^2 \qquad \text{(unitless)} \qquad (1)$$

where R is the power reflectance, and n_1 and n_2 are the real indexes of refraction of the two materials [11]. A quick calculation using Equation 1 shows that a substantial difference in the indexes of refraction is needed to obtain a high reflectance. For example, the GaAs-air interface has R = 0.31 (31%) at 980 nm. Semiconductor materials do not offer a large index difference ($\Delta n = |n_1 - n_2|$). The solution to this problem is to use a DBR with many periods.

The idea behind the distributed Bragg reflector is that the total reflectance can be increased if a series of reflecting surfaces is used. Constructive interference occurs when the initial reflected wave is in phase with subsequent reflecting waves forming a strongly reflected wavefront. Figure 3 illustrates a DBR with strong constructive interference. A DBR consists of alternating high index and low index layers. For constructive interference, the thickness of each layer needs to be $\lambda_o/4n$-thick, where λ_o is the design wavelength and n is the index of refraction of the layer. A DBR pair consists of a high and low index layer. The reflectance for a series of DBR

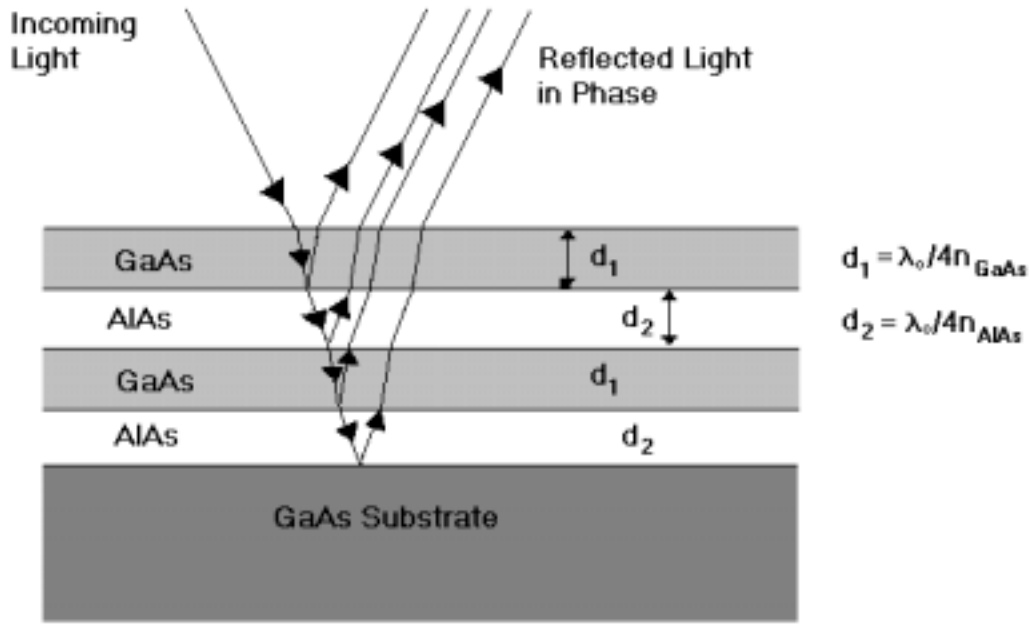

Figure 3 Illustration of constructive interference in a DBR.

pairs (valid only for integer number of pairs at normal incidence) for nonabsorbing layers is

$$R = \left[\frac{1 - \frac{n_s}{n_0}\left(\frac{n_1}{n_2}\right)^{2m}}{1 + \frac{n_s}{n_0}\left(\frac{n_1}{n_2}\right)^{2m}} \right]^2 \qquad \text{(unitless)} \qquad (2)$$

where n_s is the index of refraction for the substrate, n_o is the index for the incident medium, n_1 and n_2 are the indexes for the high and low layers, and m is the number of DBR pairs [12].

As the number of DBR pairs increase, the total reflectance will also increase as shown in Figure 4. Aluminum arsenide (AlAs) and GaAs are the most common materials used for the DBRs because of their relatively large difference in index of refraction, but more importantly because of their similar lattice constants. The similar lattice constants allow many AlAs/GaAs DBR pairs to be grown with very few defects.

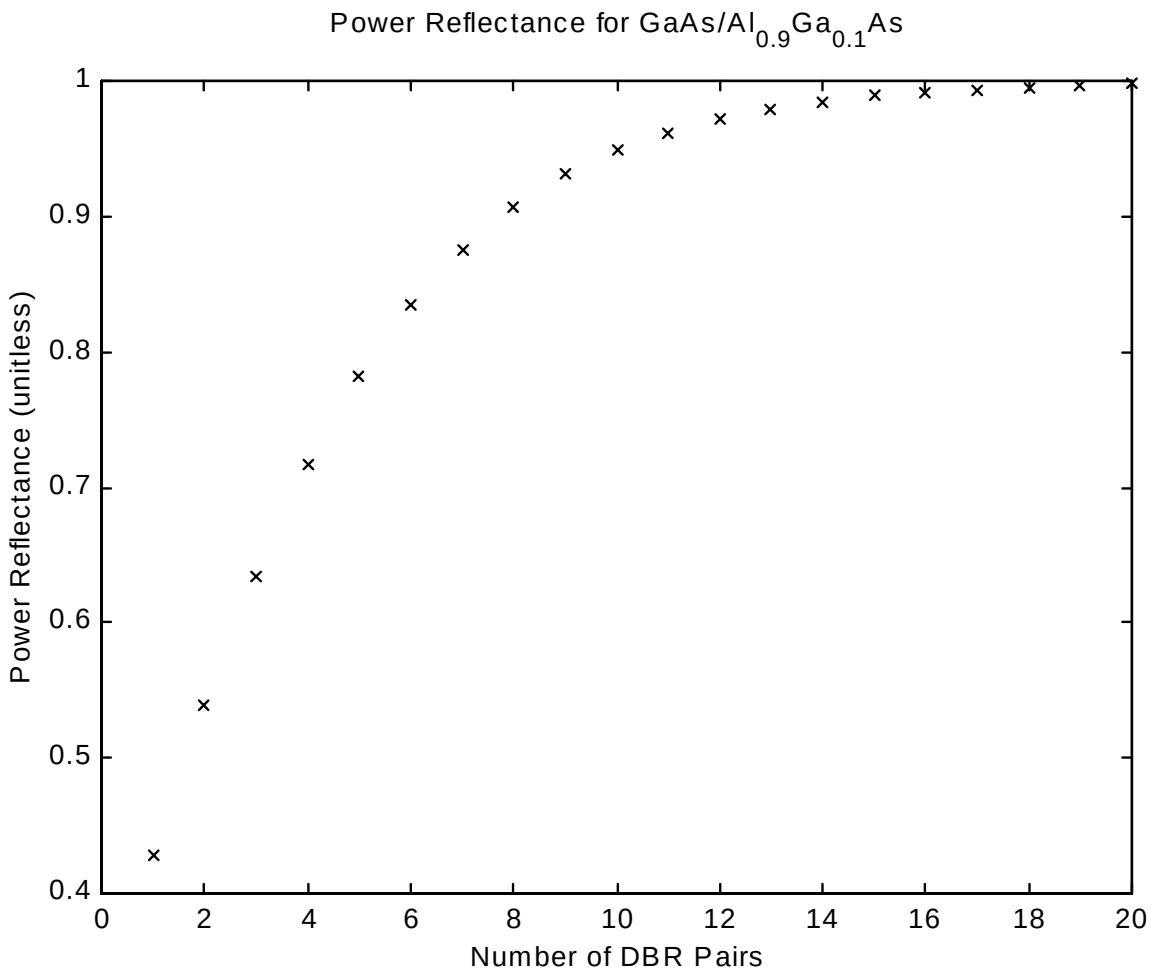

Figure 4 Power reflectance for $GaAs/Al_{0.9}Ga_{0.1}As$ DBR pairs with air as the incident medium and GaAs as the substrate.

2.2.2 Microcavity Active Region

A VCSEL operates by generating light in a narrow gain region of the device, usually in quantum wells. The microcavity is the resonant cavity of the VCSEL and contains the quantum wells. The microcavity is extremely small, typically only a few λ thick. To obtain resonance in the microcavity, the thickness of the microcavity must be an integer multiple of $\lambda_o/(2n_{\mu c})$, where λ_o is the design wavelength and $n_{\mu c}$ is the index of refraction of the microcavity.

2.3 Addressable Arrays

Two types of two-dimensional VCSEL arrays have been fabricated. The individually addressable array and the matrix addressable array have both been successfully demonstrated. Several groups have fabricated matrix addressable VCSEL arrays by directly growing the devices onto a GaAs substrate [13][14][20]. Prather fabricated an 8 x 8 individually addressable VCSEL array integrated with a CMOS driver array using flip chip bonding [16]. Tuantranont et al. fabricated a MEMS/VCSEL hybrid system by flip-chip bonding an individually addressable VCSEL array with a microlens mirror array [21]. These are just a few examples of the VCSEL arrays that have been fabricated.

2.3.1 Individually Addressable Array. In the individually addressable array, each VCSEL has at least one of its own metal contacts. The most common method of design is to make one plane a ground contact for all of the devices. Contacting each VCSEL with a metal lead creates the positive voltage to the device, thereby allowing each device to be operated independently. As a result, any single device, all of the devices, or any combination of devices can be turned on at the same time. The drawback for the individually addressable array is that for an N-by-N array, N^2 metal lines are required. Array sizes are thereby seriously limited by the number of metal lines and bond pads that can be placed onto the wafer. Figure 5 shows the comparison of an individual and a matrix addressable 8x8 array.

2.3.2 Matrix Addressable Array. For the N x N matrix-addressable array, N metal lines run horizontally across the structure to make up either the ground or positive contact, while the other contact is made of N metal lines that run vertically across the device. For the matrix addressable array, only 2N metal lines are required. At each intersection of the lines, a VCSEL is placed, so that the device has both contacts connected to it. When the lines are active, all devices that are

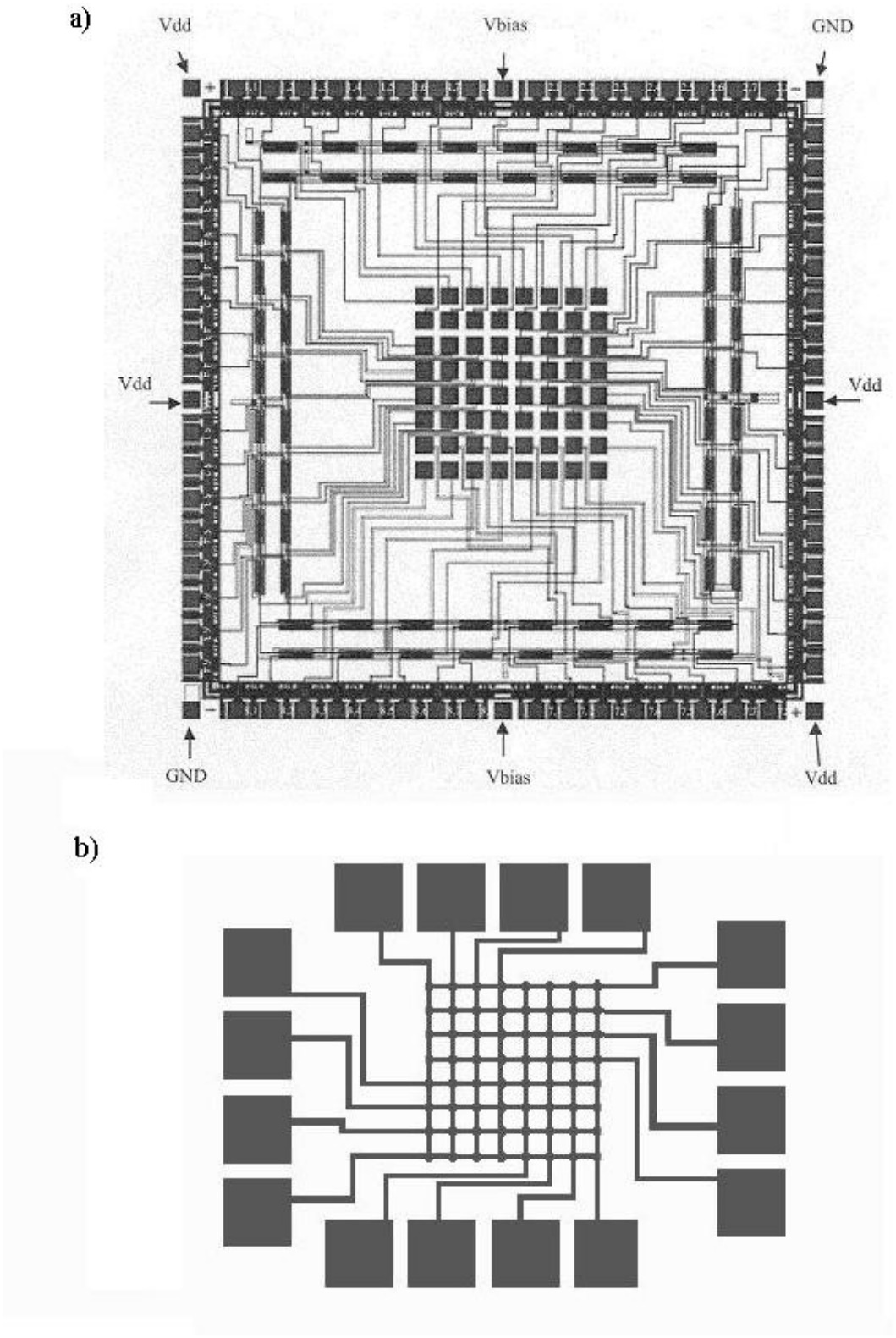

Figure 5 Comparison of an a) individually addressable array [10] and a b) matrix addressable array. Forty-eight additional lines and bond pads are required for the individual array.

at an intersection of two active lines will be turned on as demonstrated in Figure 6. The problem regarding the matrix addressable array is the inability to have complete control over the VCSELs when more than one is required to be activated. The matrix addressable array only allows control for a single VCSEL, any number of VCSELs in a single column or row, or all of the VCSELs.

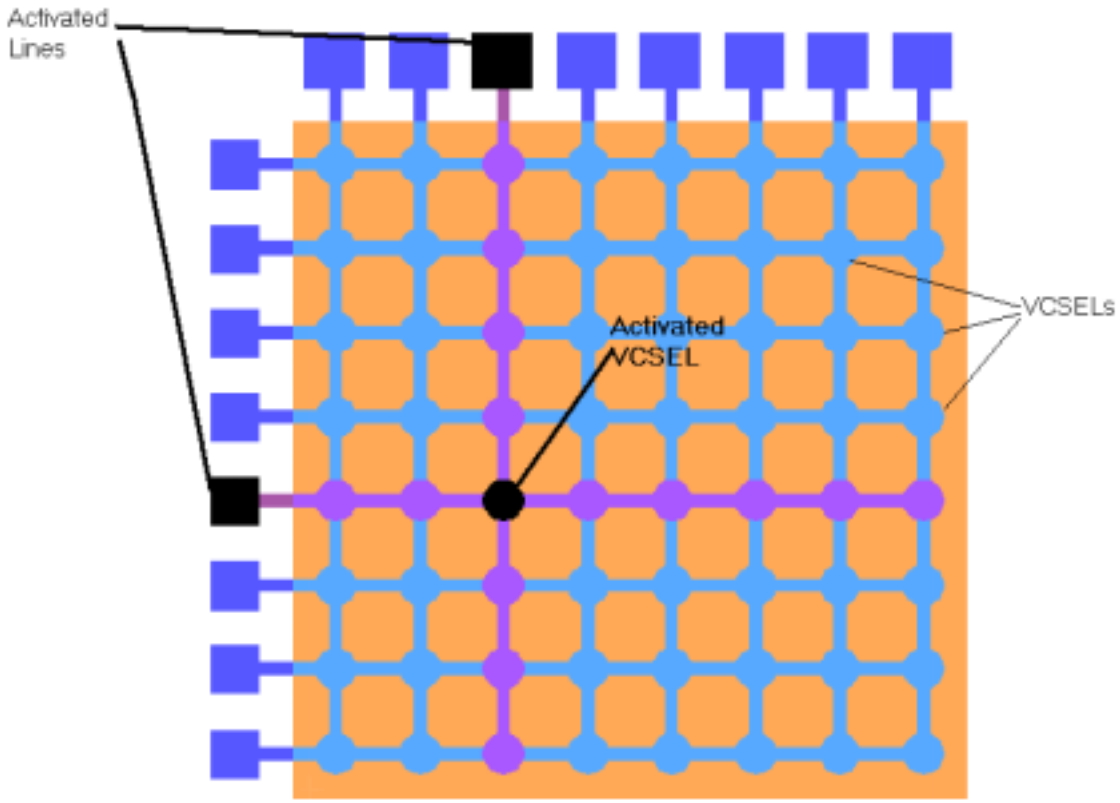

Figure 6 Matrix addressing.

In VCSEL array structures, the limiting factor in the number of VCSELs is the number of metal connections or wires that is required to operate the VCSELs. Matrix addressable arrays greatly reduce the number of metal lines that are required for the array. In comparison, for an 8 x 8 array, 64 metal lines are required for the individually addressed array but only 16 metal lines are required for the matrix-addressable array. For the same number of lines that are required for

the 8 x 8 individually addressable array, a 32 x 32 matrix addressable array can be fabricated. This results in an additional 960 VCSELs that can be placed in the array.

The technique that has been used to fabricate the matrix addressable array is to heavily dope a GaAs layer. The doped layer functions as the bottom metal contact. The device material is then grown and patterned on top of the doped layer. Next, ions are implanted between rows of devices in the doped GaAs layer. The ions neutralize regions of the n^+ doping and create an insulating layer between rows of the doped GaAs layer [13]. Finally, metal column lines are routed across the device to create the other metal contact. Figure 7 shows a schematic of this design. The heavily doped GaAs rows sit on a semi-insulating GaAs substrate and have a much higher resistivity than gold. The resistivity of these GaAs rows is a limiting factor for the size of the array.

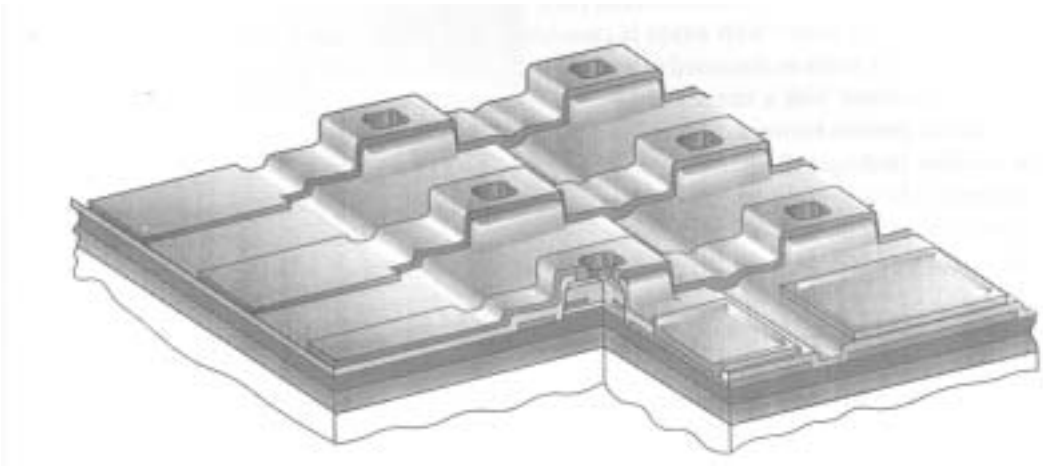

Figure 7 Schematic cross-section of a matrix addressable VCSEL array design [13].

2.4 Integration of III-V Materials with Other Substrates

The ability to integrate micro-devices from one wafer to another is thought to be a critical requirement to fabricate a matrix addressable array using gold lines. The devices can not be

grown directly on top of the gold, so they must be transferred. This type of hybrid integration has many benefits such as the ability to combine microelectronic circuitry with optical devices and has been successfully demonstrated with a variety of fabrication techniques.

Integrating III-V compound semiconductor devices with silicon substrates is a difficult task. The simplest approach has been to grow the structure in a monolithic process. However, heteroepitaxial growth of GaAs on Si produces unreliable devices [24]. The process suffers from lattice mismatch between the materials, which results in many dislocations and often poor device performance. The other approach is to grow the two materials separately and then place the III-V devices onto the Si substrate. Because of the extremely small size of the devices and materials, one cannot simply pick up the devices and place them onto the substrate. With ordinary objects, gravity is the dominating force. However, on the micrometer scale other forces, mainly adhesive forces, become significant. Adhesive forces are due to surface tension, van der Waals forces, and electrostatic forces [2]. These forces can cause the devices to stick to gripper tools rather than simply dropping when released. In addition, this method is too time consuming in order to fabricate a dense array of devices. Three approaches have been developed that avoid these problems. Fluidic self-assembly, flip chip bonding, and epitaxial lift-off offer the ability to integrate III-V optical devices with silicon.

2.5 Selective Oxidation

One of the fundamental fabrication steps in all of the integration methods is the removal of the devices from the substrate. The ability to separate the GaAs epitaxial layer from the GaAs bulk substrate is achieved through the selective oxidation of epitaxial AlAs and AlGaAs layers. Researchers at the University of Illinois developed an aluminum oxide (AlO) that was mechanically stable and had a low index of refraction, unlike other gallium and arsenide

oxides [1]. The conversion of the epitaxial AlAs or AlGaAs layers to the oxide (AlO or AlGaO) is achieved by introducing a water vapor to exposed surfaces of AlAs or AlGaAs at high temperatures [1]. The oxide can then be selectively etched using hydroflouric acid or potassium hydroxide, freeing the epitaxial layer from the substrate. Figure 8 shows the oxidation rates for varying AlAs mole fractions, thicknesses, temperatures, and times.

Additionally, the oxidation of AlGaAs has significantly enhanced the performance of VCSEL devices through the use of oxide apertures. The oxide is a dielectric and forms an abrupt oxidation front. By oxidizing the AlGaAs layer so that only the AlGaAs in the middle of the device remains, carriers are forced into this region when the device is turned on. Figure 9 illustrates oxidation of the AlAs and GaAs layers. Active regions of a few microns can thereby be defined providing optical confinement and the ability to operate in a single mode. VCSEL structures that have utilized the oxide aperture have demonstrated record low threshold currents and voltages along with record power conversion efficiency [1].

2.6 Fluidic Self-Assembly

Fluidic self-assembly (FSA) of GaAs microstructures onto silicon substrates has been studied and attempted by several research groups [20] [21][24][25]. FSA offers the potential of mass integration of GaAs structures with Si substrates in a simple process. The problem with FSA is that it lacks precise control of placement of the devices. It has had limited success rates with VCSEL devices. Two approaches of FSA have been developed. The first relies mainly on gravitational forces for assembly with preferential assembly achieved through the shape of the devices and the receptor sites, while the second relies on capillary forces for self-assembly.

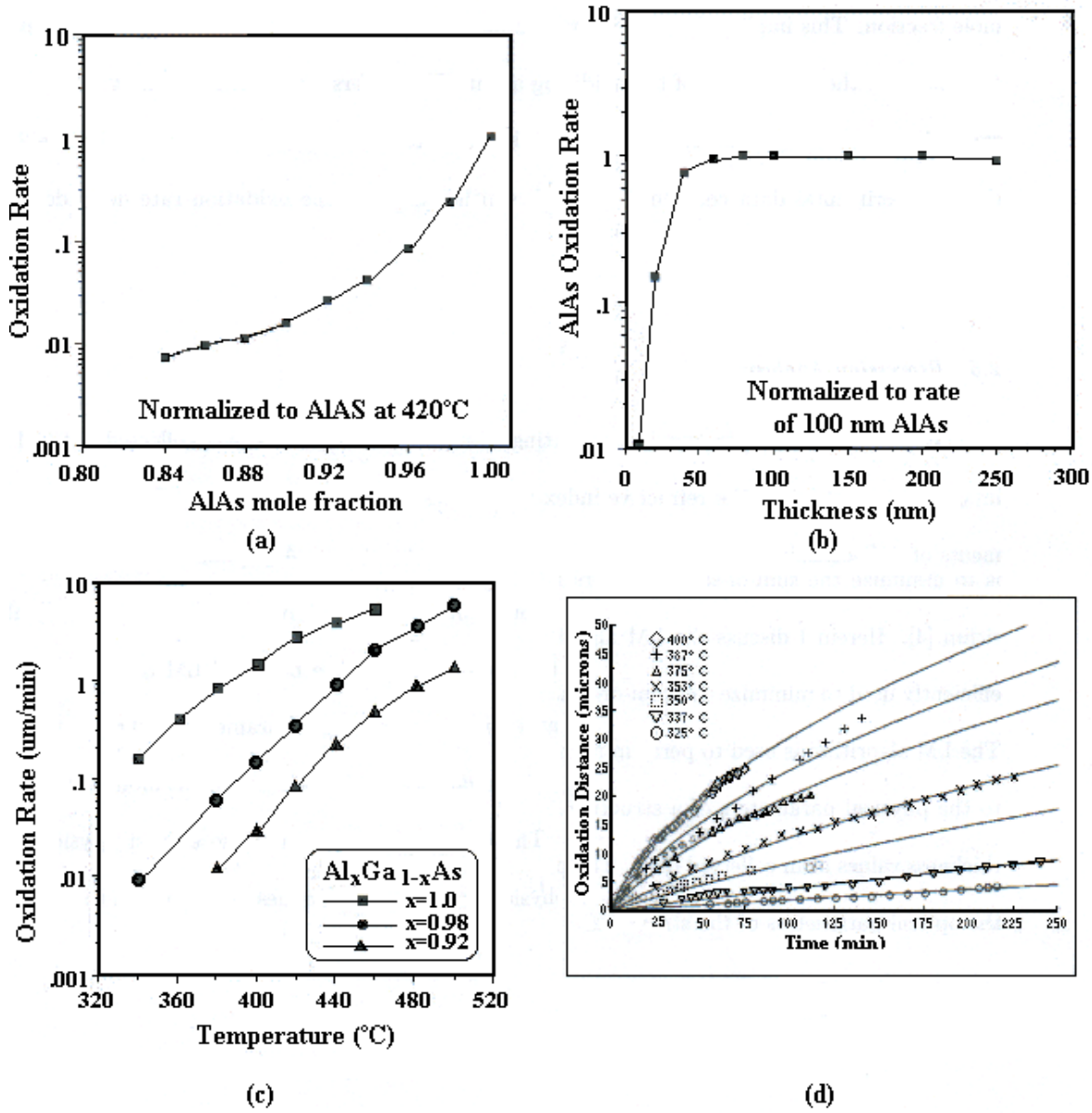

Figure 8 Oxidation rate dependence on a) AlAs mole fraction, b) layer thickness, c) temperature, and d) time [1].

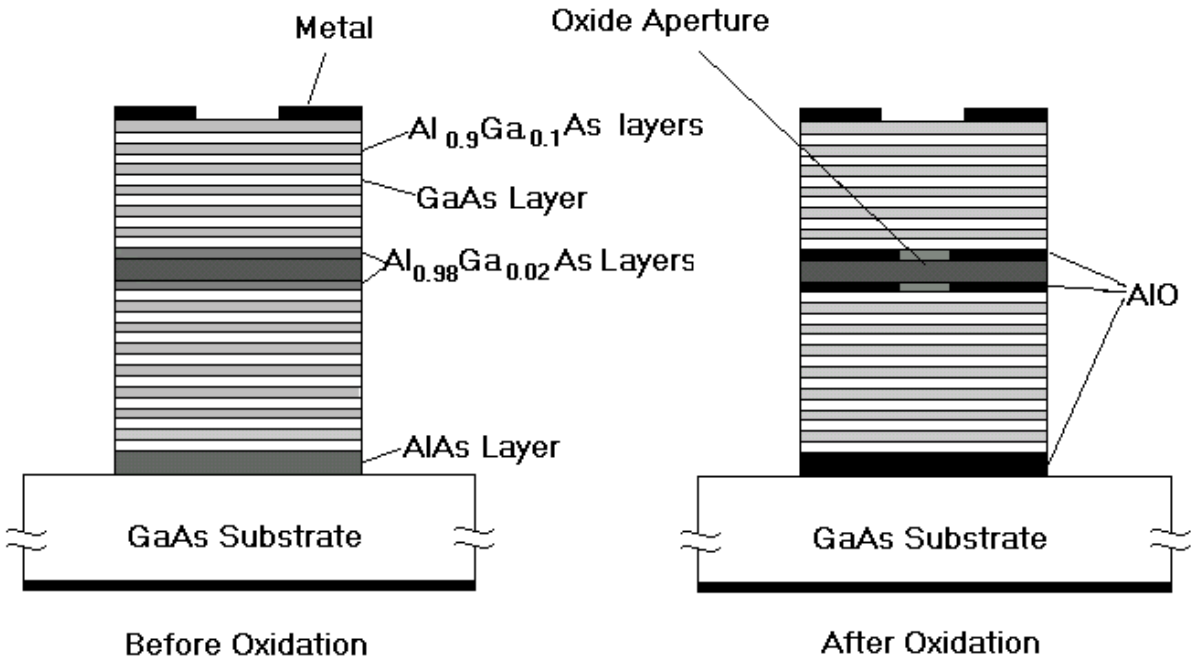

Figure 9 Before and after oxidation for a lift-off VCSEL.

In the first approach, the FSA process begins by growing the VCSEL material and an underlying aluminum arsenide (AlAs) sacrificial layer on the GaAs substrate [21]. A metal layer is deposited on top of the VCSEL to form one of the contacts. Ion milling is used to etch the VCSEL structures down to the AlAs layer with 68˚ sidewalls [25]. The next step is to pattern the silicon substrate. A hole is created in the Si substrate to act as a receptor site for the VCSEL. A wet anisotropic etch is used to form the hole. Due to the arrangement of atoms in the silicon lattice, silicon can be etched in one crystal direction much faster than others. Ethylenediamine pyrocatechol etches silicon with greater than 100:1 selectivity over the {111} planes [25]. A trapezoidal hole can be formed with a 54.7˚ sidewall [17]. The next step is to release the VCSEL devices grown on the GaAs substrate. A buffered hydroflouric acid selective etch is used to remove the AlAs sacrificial layer, which frees the devices from the GaAs substrate [20]. The devices are then placed into a carrier fluid of either methanol or ethanol [25]. The fluid with the

devices is then dispersed over the silicon substrate. The trapezoidal shape of the device causes the VCSELs to preferentially fall with the small side down due to viscous forces. A metal ring is then deposited on top of the VCSEL to form the topside contact. Figure 10 demonstrates this process. Researchers at U. C. Berkeley have demonstrated successful fill rates of 70% when integrating VCSELs onto Si substrates [5].

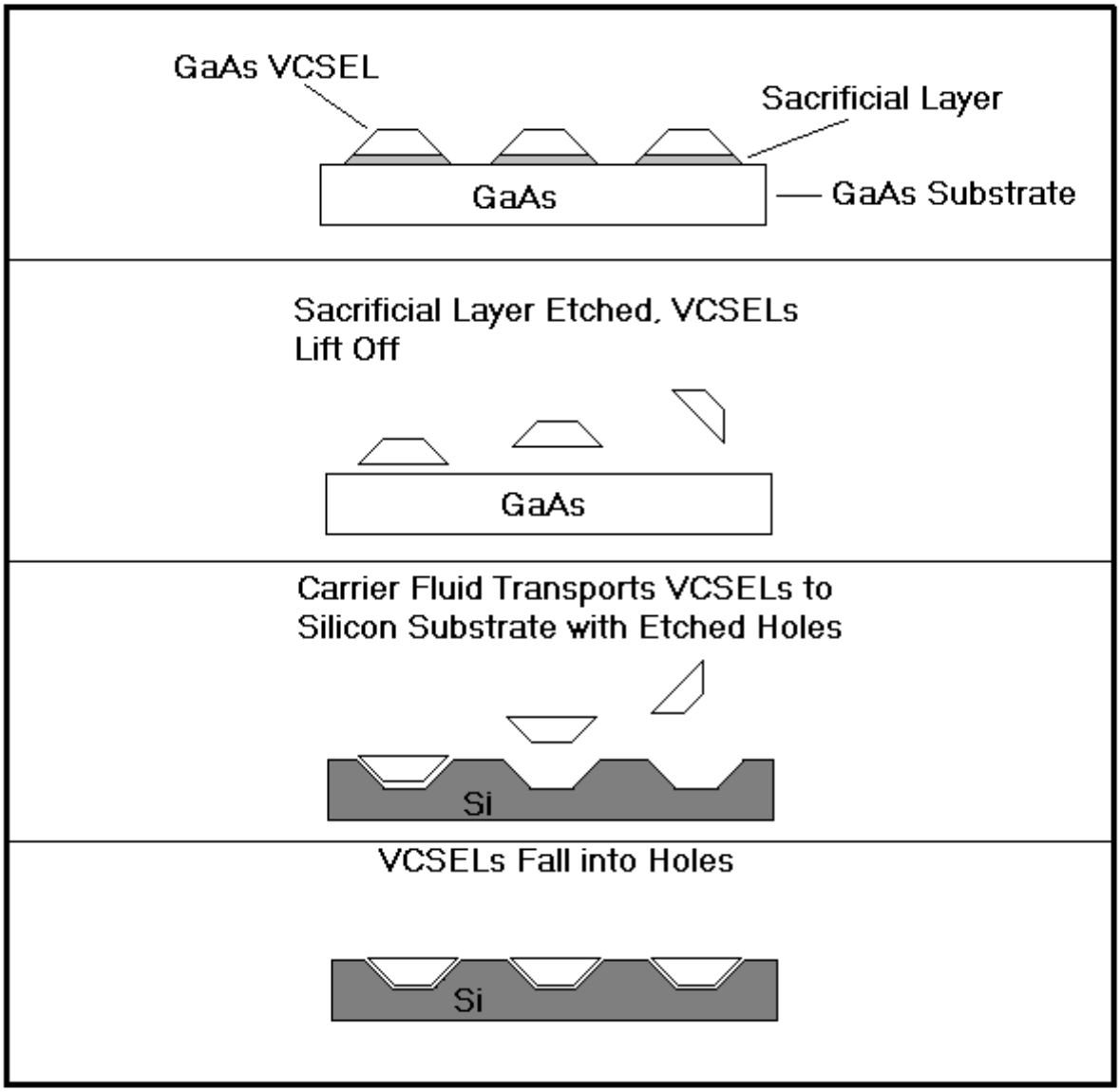

Figure 10 FSA process for integration of GaAs VCSELs with a Si substrate.

While this method of FSA of VCSELs onto silicon substrates has relied on gravitational forces for assembly, capillary forces have been demonstrated to self-align larger devices using FSA [18]. With the MUMPs® process, angled sidewalls cannot be formed. Without the trapezoidal shape, the VCSELs will not preferentially fall with the correct orientation into the proper hole in the Si substrate. Success rates will then be substantially reduced. However, with chemical processing of the VCSEL and the silicon substrate, capillary forces can be used to self-align the VCSEL into holes in the Si substrate. A 100% success rate of structures with a radius of 50 μm falling into specific areas onto a Si substrate through FSA has been achieved through capillary action [3].

Additional processing of the structures and the substrate introduces an attractive force between the receptor site and a surface of the device structure. The FSA technique utilizes hydrophobic (repelled by water)–hydrophilic (attracted to water) surface patterning and capillary forces of an adhesive liquid between binding sites to self-align the device [18]. The first step in the process is to deposit a gold layer onto both the device and the substrate. The gold is then patterned so that there is only gold on surfaces where bonding is desired. Gold is naturally hydrophilic as is the Si substrate [18]. However, by soaking the substrate with the patterned gold in ethanolic alkanethiol, a monolayer is formed on the gold patterns making the gold hydrophobic, while the Si substrate remains hydrophobic. Next, the substrate is passed through a film of a hydrocarbon-based liquid adhesive and then into water. The adhesive selectively coats the binding sites (gold regions) on the wafer. Only the substrate is lubricated so that the structures do not bond to themselves when suspended in the carrier fluid. The devices are then immersed into the water and directed toward the substrate with a pipette. After the gold hydrophobic regions of the microstructures come into contact with the adhesive coating, the

microdevices self-align due to interfacial free energy minimization between the surfaces [3]. The adhesive, polymerized at 80˚C for half an hour permanently bonds the structures to the binding site [18]. Figure 11 illustrates the self-alignment process.

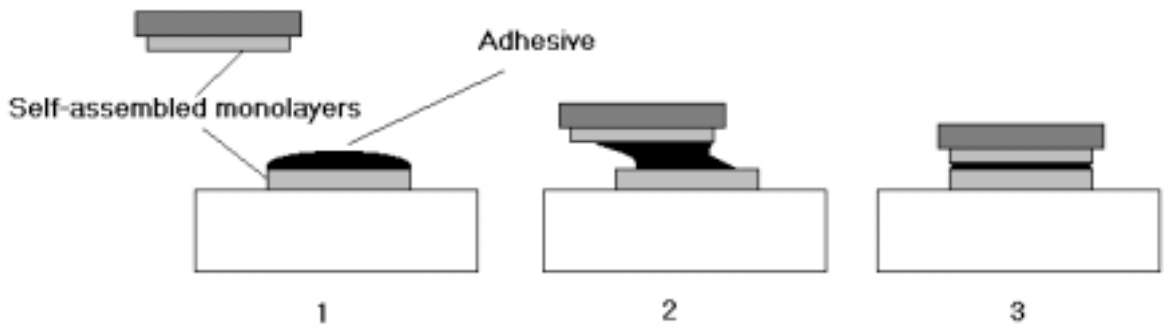

Figure 11 Self-alignment utilizing capillary forces

2.7 Wafer to Wafer Transfer

While FSA relies on removing the devices from the GaAs substrate and transferring them onto the Si wafer, other techniques have been developed that integrate the GaAs devices with the Si wafer by bonding the wafers together and then removing the GaAs substrate. By transferring the devices while still on the wafer, the concern that devices will fall correctly into place with a certain orientation is eliminated. One can precisely control the placement of the devices, however, the process is complicated by this critical alignment step. Both flip-chip bonding and epitaxial lift-off are wafer to wafer transfer techniques that use similar approaches.

In both techniques, the devices can be fabricated before (pre-processing) or after (post-processing) the epitaxial layer has been transferred to the other substrate [15]. The advantage with post-processing is that critical alignment between the wafers is not necessary. The wafers can be bonded together and the devices fabricated. In pre-processing the devices are fabricated and then the wafers must be precisely aligned, to ensure that the devices are placed properly onto

the Si wafer. The problem with post-processing is that metal surfaces are necessary for bonding. To fabricate matrix addressable arrays, each metal line must be electrically isolated. With post-processing, electrical isolation is not assured. Consequently, pre-processing is required and alignment cannot be avoided.

2.7.1 Flip-Chip Bonding. Flip-chip bonding (FCB) is a technique that has been used since the 1960's to integrate microelectronic components [7]. Recent work by a few groups has illustrated the effectiveness of this technique in integrating GaAs VCSELs with Si substrates. Prather has successfully flip-chip bonded an 8x8 individually addressable VCSEL array onto a CMOS driver [8]. Tuantranont et al. has also demonstrated the success flip-chip bonding. This group developed a MEMS/VCSEL hybrid system that integrates an individually addressable VCSEL array with a MEMS-controllable microlens array [22].

In the flip-chip bonding approach, a GaAs epitaxial layer is first grown on a GaAs substrate. The epitaxial layer contains an underlying etch stop layer or sacrificial layer, depending on the method of substrate removal. The epitaxial layer is then patterned and metal contacts are placed on both the epitaxial GaAs layer and on the Si substrate. Gold bumps (small balls of gold) are placed on the metal contacts of the substrate. The wafers are then aligned and bonded together using a bump bonder machine. After the wafers are bonded, the next step is to remove the excess substrate. This can be accomplished by grinding the wafer down using chemical mechanical polishing. Once most of the wafer has been removed, a chemical etch can be used to remove the remaining portion. The etchant will (or will virtually) cease etching once it reaches the etch stop layer. The other approach is to use a selective etchant that only erodes the sacrificial layer. Once the sacrificial layer is removed the GaAs substrate will come off. The devices will remain on the Si substrate. Figure 12 outlines the flip-chip process.

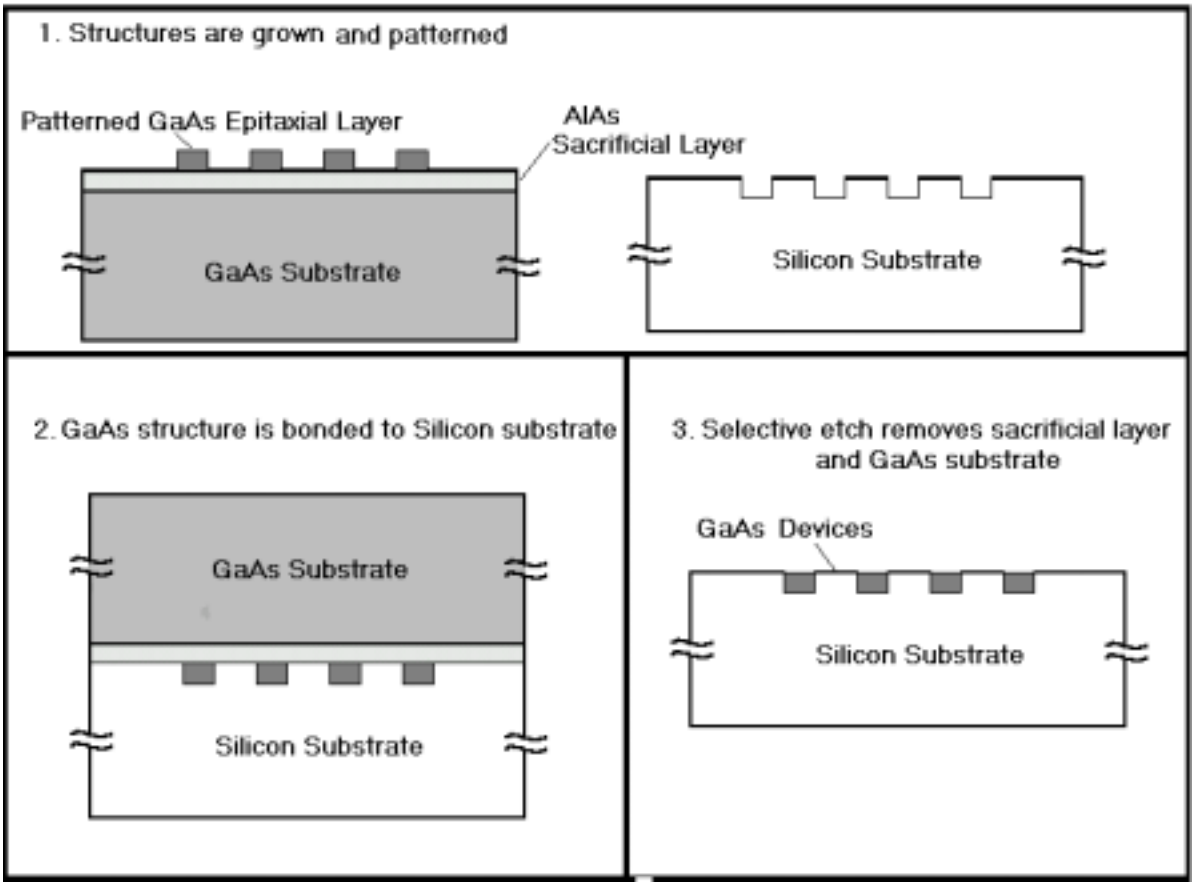

Figure 12 Flip-chip bonding of GaAs epitaxially grown VCSELs onto a Si substrate.

2.7.2 Epitaxial Lift-Off. Epitaxial lift-off (ELO) is another viable integration technique that has been successfully demonstrated by several research groups [5][15]. In the ELO process, devices are transferred from one substrate to another by removing a sacrificial epitaxial layer from the host wafer. Next, the remaining epitaxial layers are transferred to the target substrate. The ELO process allows for precise alignment of the devices because the devices are fixed on the epitaxial layer when they are transferred to the Si substrate.

The first step in the ELO process is to grow a thin film GaAs epitaxial layer and an underlying sacrificial AlAs layer on the GaAs host substrate [8]. The epitaxial layer can then be

processed along with the Si substrate to fabricate the devices and create the receptor sites. The epitaxial layer is then separated from the substrate by etching away the sacrificial layer. Since the epitaxial layer is very thin, it can suffer from strain and is extremely fragile. To eliminate or reduce the strain incurred and increase the mechanical strength, a layer of wax can be placed on top of the thin film heterostructures before the substrate is removed [5]. The thin film is then aligned and bonded to the Si substrate. After bonding the wax is removed

2.8 MEMS

Micro-electro-mechanical systems (MEMS) are miniaturized electronic and mechanical components. Bulk micromachining, surface micromachining, and LIGA (Lithographie, Galvanoformung, Abformung) techniques are used to create these microstructures [4]. Bulk micromachining is processing that removes portions of the substrate while surface micromachining is processing on top of the substrate [11]. LIGA, meaning lithography, electroplating, and molding, is a micromachining process that is capable of yielding structures with high aspect ratios [11]. Mechanical devices such as beams, pits, gears, membranes and even motors have been fabricated using LIGA for a variety of applications that have mainly included sensors and actuators [4]. MEMS devices offer the obvious advantage of miniaturization, which saves space, energy, and weight, but they also have the potential to reduce cost since thousands of these devices can be fabricated on a single wafer. The ability to integrate micro-optical devices with MEMS structures offers many potential advantages. For example, it is possible to construct a MEMS-tunable VCSEL or place a VCSEL onto a polysilicon-MEMS micromirror and steer the VCSEL's beam output.

2.4 MUMPs®

The MUMPs® (Multi-User MEMS Processes) uses a three-layer polysilicon micromachining process to fabricate MEMS structures [9]. The foundry MUMPs® process uses a set growth sequence of silicon dioxide, polysilicon, and metal. The user designs the MEMS layer structures and sends the design to the MUMPs® foundry. The advantage of using MUMPs® is a reduction in cost since a foundry completes the fabrication from a user's design. The disadvantage is that the user is limited by the standard MUMPs® layer thickness and order of layers.

The MUMPs® process starts by using an n-type (100) oriented silicon wafer [9]. The process includes low-pressure chemical vapor deposition to deposit the subsequent polysilicon (poly) and silicon dioxide (oxide) layers. MUMPs® structures can have up to seven different layers including polysilicon (poly0, poly1, and poly2), silicon dioxide (oxide1 and oxide2), nitride, and gold (metal) [9]. Table 1 lists the different layers and their thicknesses.

The nitride layer acts as an electrical isolation barrier between a silicon substrate and the subsequent polysilicon layers. The oxides, which are actually phosphosilicate glass, are used as sacrificial layers. Various masks are used to pattern the different layers and a reactive ion etch is used to remove the unwanted layers. Table 2 lists the different etches and their optimum depths. The user, with a computer aided tool, specifies which different etches he/she wants and the precise location he/she wants the etch to be performed. By defining different lithography steps, various MEMS structures can be created through the MUMPs® process.

Table 1 MUMPs® Layers and Thickness [6]

Layer	Thickness (μm)
Nitride	0.6
Poly 0	0.5
Oxide 1	2.0
Poly 1	2.0
Oxide 2	0.75
Poly 2	1.5
Metal	0.5

Table 2 MUMPs® Lithography Options [9]

Layer to be etched	Lithography name	Depth (μm)
Oxide 1	Dimple	0.75
Oxide 1	Anchor1	2.0
Oxide 2	Poly1-Poly2 Via	0.75
Oxide 2	Anchor 2	2.75

2.10 Summary

In this chapter, VCSEL structures and their operation were presented. An introduction to MEMS and the MUMPs® process was given. Matrix addressable and individually addressable VCSEL arrays were presented and compared. Finally, the integration of optical III-V devices with silicon MEMS was outlined by discussing the FSA, ELO, and FCB fabrication techniques.

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3. Design Methodology

3.1 Introduction

In this chapter, I discuss the three main design elements of my thesis. The first item discussed is the design of the VCSEL structure and the numerical modeling of the device. The next design issue outlined in this chapter is the prototype photomasks that were designed to conduct the experiments. Finally, I present a MUMPs® foundry design useful for studies of micro-optical device arrays.

3.2 VCSEL Design

Two different designs were created, a bottom emitting and a top emitting VCSEL device. The VCSEL was designed to operate at a wavelength of 980 nm on a GaAs (100) oriented substrate. The DBR consists of alternating 638 Å $Al_{0.9}Ga_{0.1}As$ low index layers and 516 Å GaAs high index layers plus graded interfaces. The thickness of a low (L) and high (H) index layer plus two 180 Å graded interface segments is equivalent to an optical thickness of a quarter wavelength. Digital super-lattice (SL) graded DBR interfaces were used to approximate a linear grade over a 180 Å-thick segment between each H-L pair. The linear grade is used to reduce electrical resistance in the structure. The VCSEL contains three 80 Å-thick $In_{0.2}Ga_{0.8}As$ quantum wells. Two 206 Å-thick $Al_{0.98}Ga_{0.02}As$ layers within two of the $Al_{0.9}Ga_{0.1}As$ DBR layers next to the VCSEL function as oxide apertures. A 3290 Å-thick AlAs bottom layer was grown to serve as the oxide lift-off layer for the VCSELs. Two 1220 Å-thick $Al_{0.5}Ga_{0.5}As$ layers were used as adjustment layers.

3.3 VCSEL Modeling

I performed numerical modeling of the VCSEL device with the structure layout specified in the previous section using MATLAB. The model includes calculations for power reflectance, reflectivity phase, real index of refraction, and electric field intensity.

In the first part of the modeling, I calculated the power reflectance and the reflectivity phase of the VCSEL structure looking down on the structure as the wavelength is varied. Figure 13 shows the results. In the plot of the power reflectance, the important thing to notice is the high reflectance around the design wavelength of 9800 Å. However, the reflectance right at the design wavelength drops off sharply. The Fabry-Perot dip, the sharp drop-off, is the result of the device having a Fabry-Perot etalon structure. With the reflectivity phase, the significant property is the 2π phase shift that occurs at the design wavelength, another common attribute of VCSEL structures.

The other numerical modeling that is performed for the VCSEL device involves calculating the real index of refraction through the device and plotting the electric field intensity or standing wave at the resonant wavelength of 980 nm. Figure 14 shows the "Christmas tree" electric field present around the VCSEL. Figure 15 illustrates that the electric field intensity peak overlaps the quantum wells. This helps increase the power efficiency of the device. Figure 16 shows one of the SL-graded layers from a high index to a low index with the approximate linear grade shown as the dashed line.

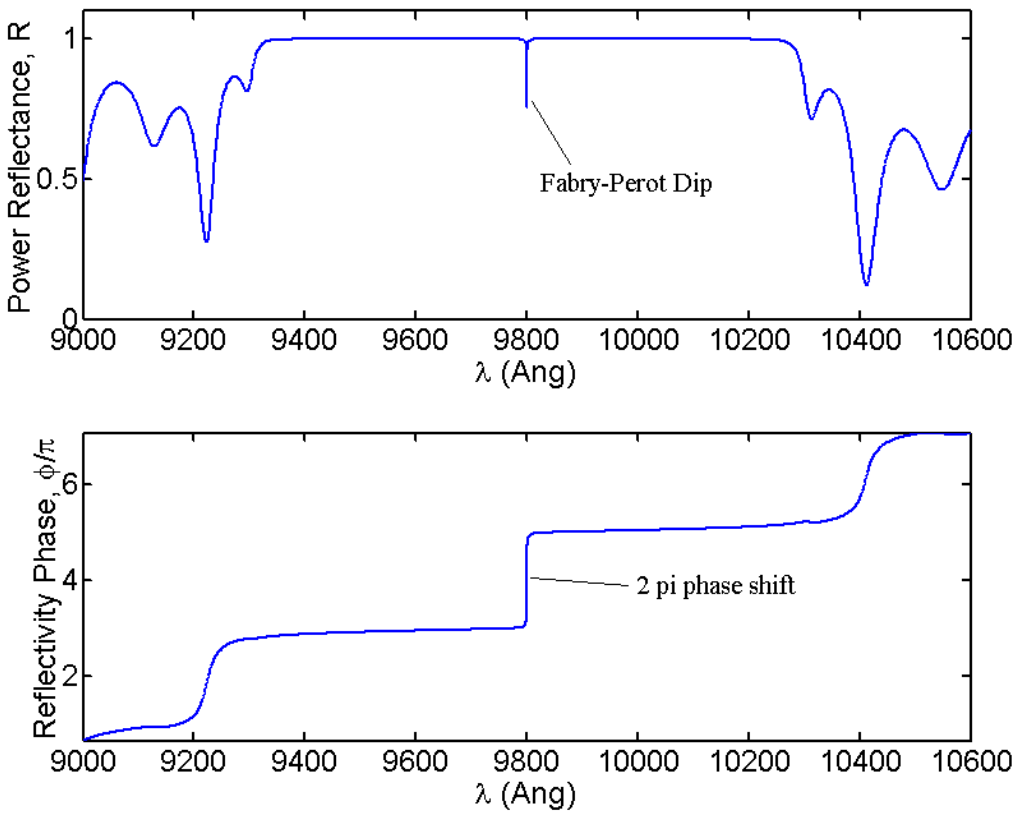

Figure 13 Power reflectance (top) and reflectivity phase (bottom) modeling of the VCSEL structure.

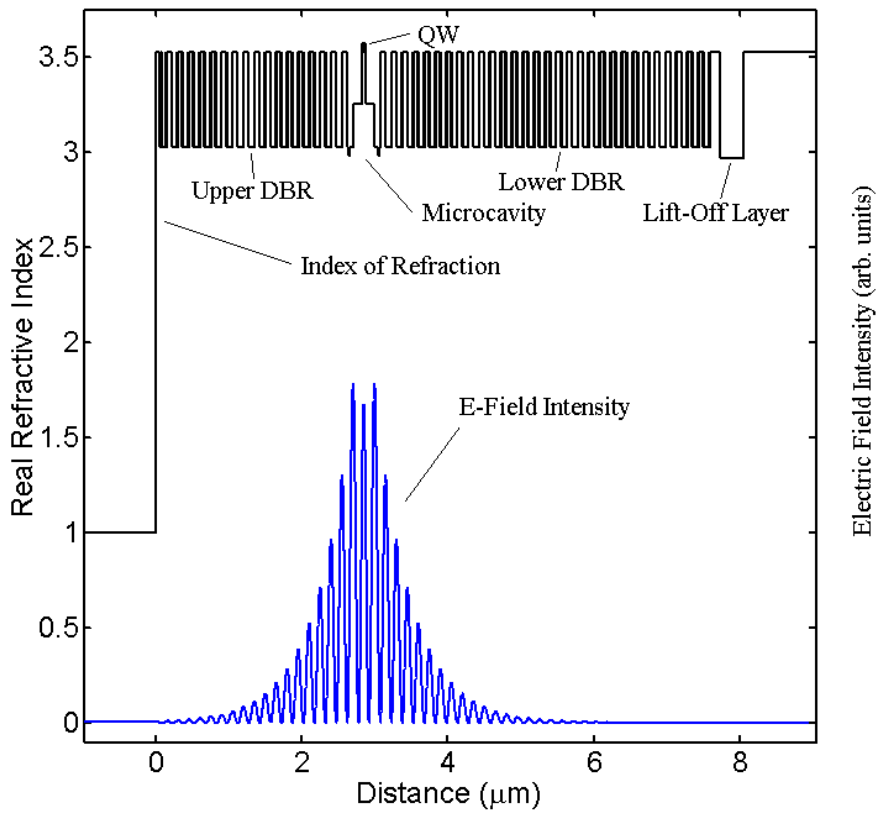

Figure 14 Modeling of electric field intensity and index of refraction in the VCSEL.

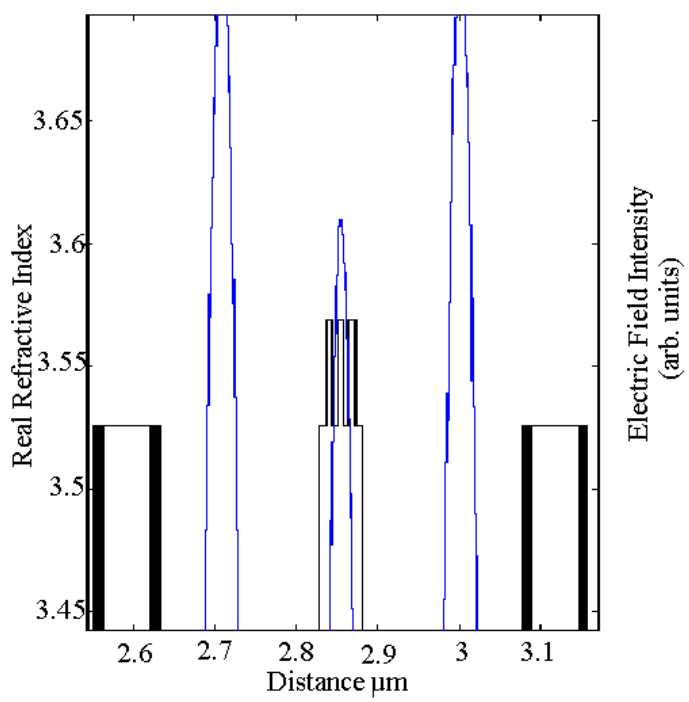

Figure 15 Standing electric field intensity modeling in the quantum wells.

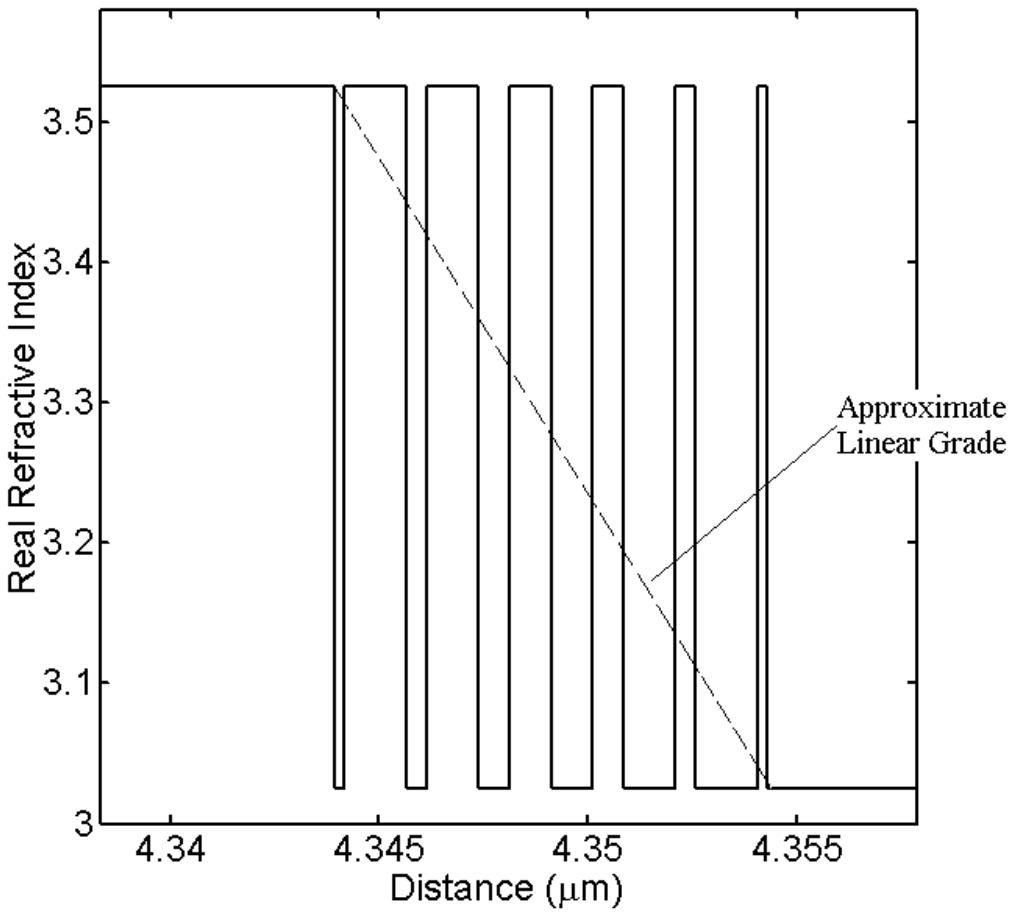

Figure 16 $Al_{0.9}Ga_{0.1}As$ and GaAs graded index layer.

3.4 Matrix Design Approaches

In designing the matrix array three different ideas were attempted to create the different heights for the metal contacts. The first approach is to etch a recess equal to the height of the device into an insulating substrate and deposit the bottom metal contact inside the recess. The device is then placed on top of the metal. Running metal lines on top of the surface of the substrate perpendicular to those lines in the recess the serve as the other contact to the device. The second idea is to deposit the bottom metal on the substrate and then spin an insulating film onto the wafer. Several films may need to be deposited to achieve the required height of the

device. Metal lines are then deposited on top of the film. The third approach is simply a combination of the first two. Metal is deposited into an etched recess. An insulating film is then spun onto the wafer. Finally, the top metal is deposited. By using this method, the problems associated with each method should be reduced. Figure 17 illustrates the three different approaches.

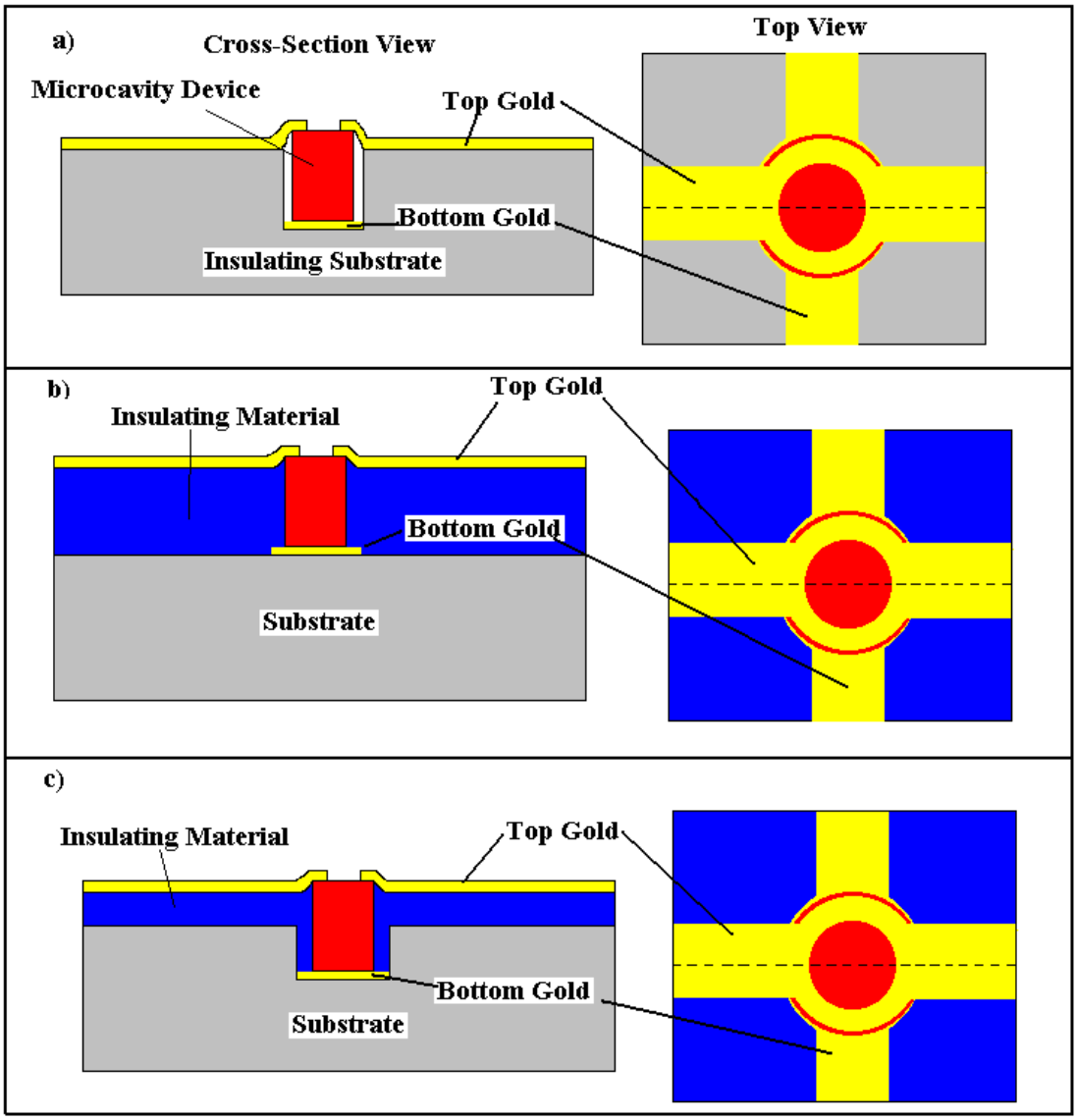

Figure 17 Illustration of three different design approaches: a) etched insulating substrate, b) spun-on insulating material, and c) combination of etched substrate and insulating material.

3.5 Photomasks

I designed photomasks for the photolithography processes that were required to study the fabrication techniques for the matrix addressable array and the VCSEL devices. Photomasks are made from clear solid materials usually either quartz or lime glass. The photomasks contain high-resolution opaque images on one side of the surface. Figure 18 shows a typical four-inch photomask made on lime glass. The photomasks are used to transfer images from the photomask to the wafer using conventional photolithographic processes, which I describe in Chapter 4. Each photomask was designed so that it could be used with positive photoresist. The dark field, or opaque region of the photomask, is the area that will be protected from the processing steps (photoresist not removed).

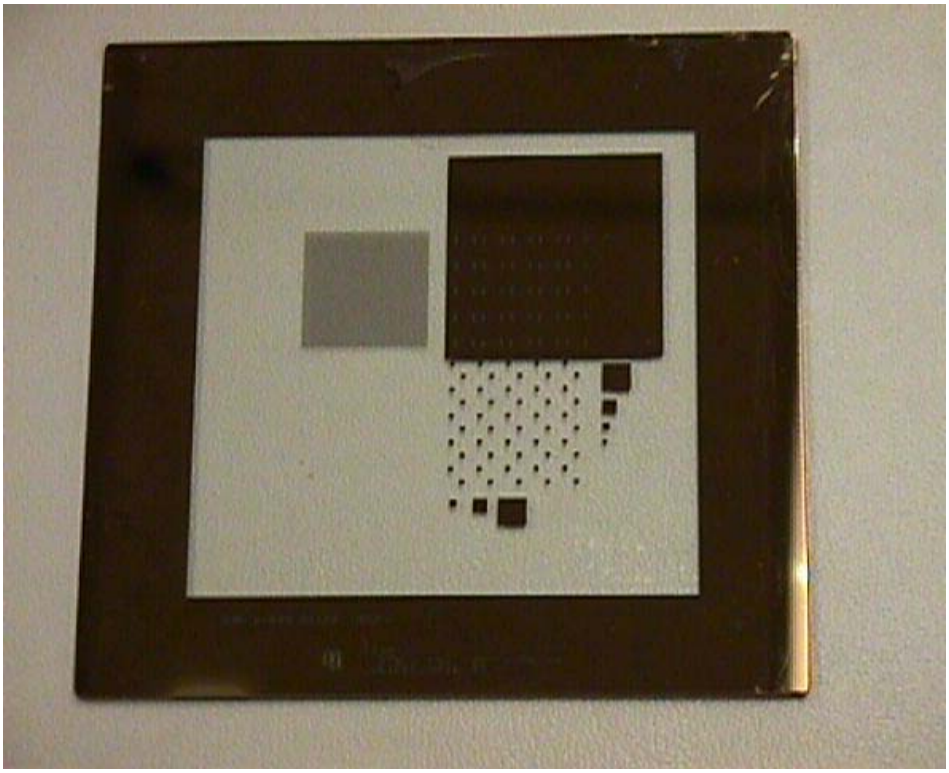

Figure 18 Picture of photomask #1.

Three separate photomasks were created, each divided into four quadrants with their own pattern. The photomasks allow for 25 separate 8 x 8 arrays to be fabricated. Each array is designed for a 20 µm diameter micro-optical device. L-Edit is the computer aided design tool that was used to layout the design of the photomasks [1]. The L-Edit files were then converted to a GDSII file and sent to the Photoplot Store in Colorado for the actual manufacturing of the photomasks [2]. Figures 19, 20, and 21 show the entire L-Edit layout for the three photomasks. Because the VCSEL devices are only 20 µm in diameter, the details of the design can only be viewed by zooming in on the masks.

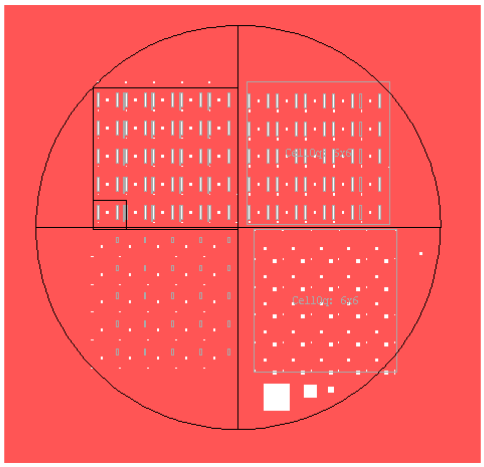

Figure 19 L-Edit layout of photomask 1.

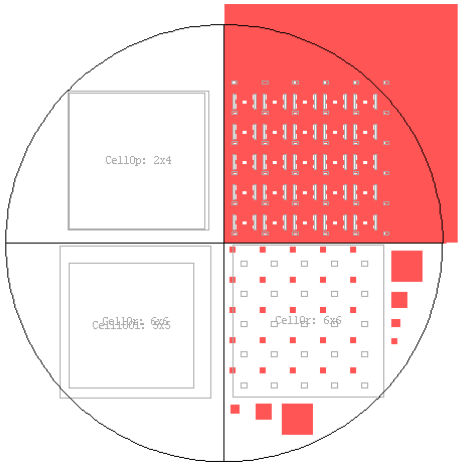

Figure 20 L-Edit layout of photomask 2.

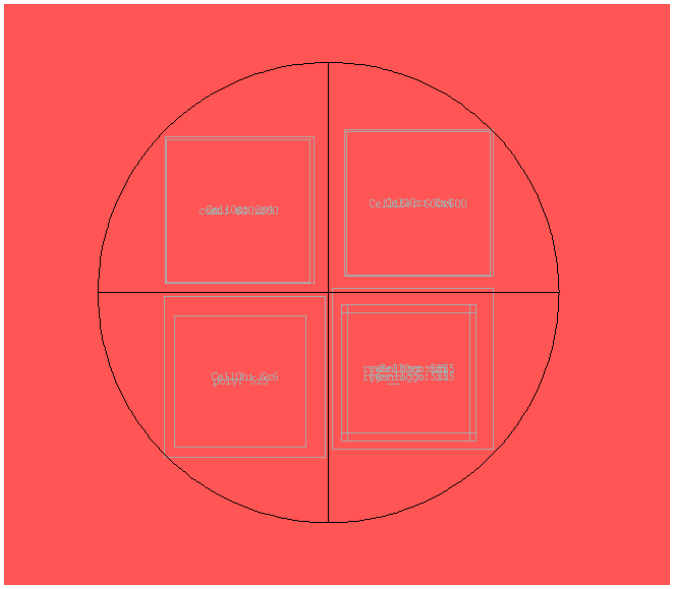

Figure 21 L-Edit layout of photomask 3.

3.6 VCSEL Photomasks

The first set of photomask layouts were designed to enable the fabrication and testing of the VCSELs. Though the wafers were grown with the VCSEL design material, mesas need to be etched to define the horizontal dimensions of each individual VCSEL. Gold contact rings are also needed to test the VCSELs to ensure they emit light. Finally, lift-off VCSELs require solid gold contacts to enable the devices to bond to the target substrate. Since two integration techniques can be investigated, FSA and FCB, separate VCSEL designs had to be created for each approach.

3.6.1 VCSEL Photomask Design for FSA. For the FSA approach, vast amount of devices need to be fabricated. Placing thousands of these devices into the carrier fluid will increase the probability that the devices will fall into the array on the target substrate. The photomask design contains an array of 600 x 600, 20 μm-diameter opaque disks. The disk centers are separated by 30 μm. With a 100% yield, the photomask will allow for 360,000 VCSELs to be fabricated in less than a square inch area of the wafer. Figure 22 demonstrates a portion of the large array.

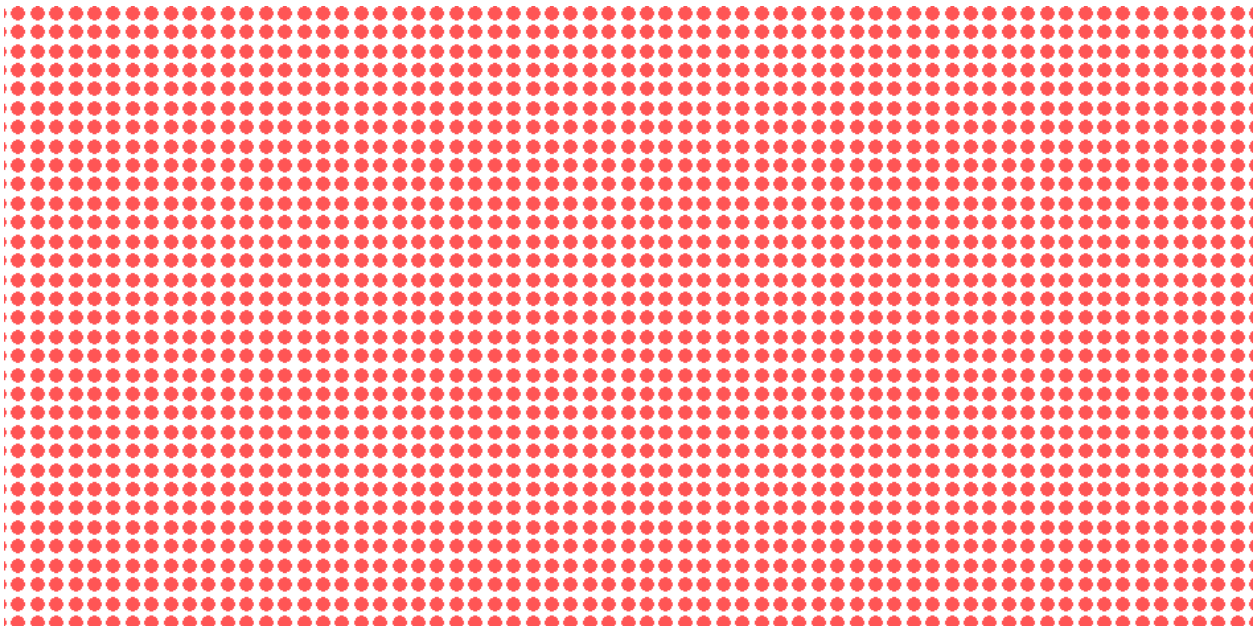

Figure 22 Design of VCSELs for FSA.

3.6.2 VCSEL Photomask Design for FCB. For the FCB approach, the VCSELs need to be designed so that they can be directly placed onto the holes of the target wafer. Therefore, 25 separate 8 x 8 arrays of 20 µm-diameter disks were created for the FCB tests. The arrays precisely line up with the photomasks that were designed to create the holes. The center of each disk in the array is 50 µm away from the center of the nearest disk. Figure 23 shows one of the 8 x 8 arrays.

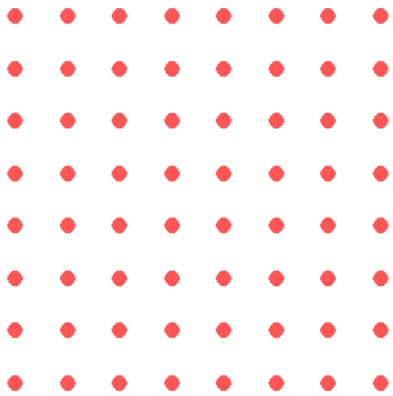

Figure 23 Mask design of 8 x 8 VCSEL array for FCB.

3.6.3 VCSEL Photomasks for Testing. Two designs were created on the photomasks so that the VCSELs could be tested while they are still on the original wafer, one for the FCB VCSEL design and one for the FSA VCSEL design. Although the lift-off VCSELs are designed to be bottom-emitting, so that when they are transferred to the target substrate they will emit away from the wafer, a few VCSELs were designed to be top-emitting so that they could be tested before transfer. To test the VCSELs a metal contact is needed on the top surface. An aperture window in the contact must be included to allow the beam to escape. The design for the contact is a ring with an outer diameter of 18 μm and inner diameter of 8 μm. The outer diameter of the ring contact is 2 μm smaller than the mesa diameter. This allows for a 1 μm edge around the VCSEL. This buffer zone will prevent metal from coating the sides of the structure and possibly shorting the device. To help remove the gold in the aperture window in the metal lift-off process, a 2 μm-thick slice is taken out of each ring. Figure 24 shows one of the gold rings and Figure 25 demonstrates one of the 8 x 8 arrays for the FCB approach.

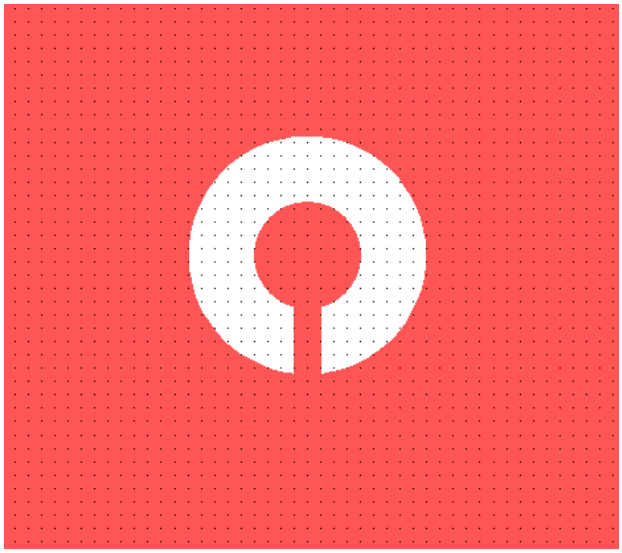

Figure 24 Ring contact design for on-wafer testing.

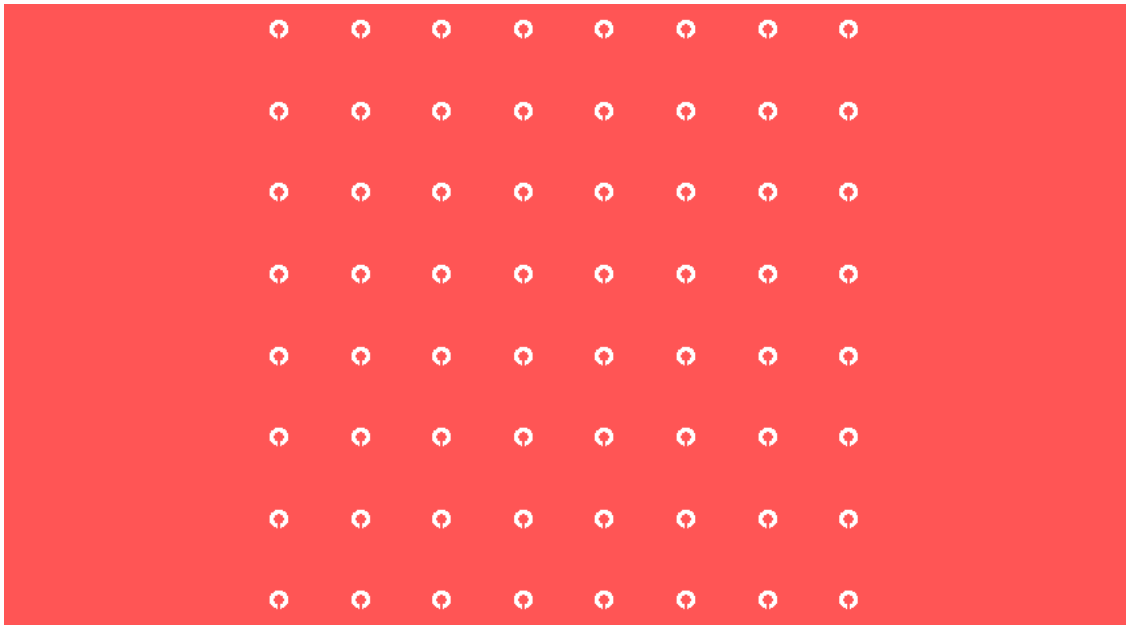

Figure 25 On wafer testing design for 8 x 8 FCB VCSEL array.

3.6.4 Photomask Design for Bonding Contact. A solid metal contact must be placed on the VCSEL structures before lift-off so that the VCSEL will stick and, after heating, bond to the target substrate. Again, a 1 µm buffer zone is required to assure that the metal does not fall onto the sides of the VCSEL. Therefore, the disk has a diameter of 18 µm. Again two designs are completed, one for FCB which contains twenty-five separate 8 x 8 arrays and one for FSA which is one 600 x 600 array. Figure 26 shows the design for one of the 8 x 8 FCB arrays.

3.7 Photomask Design for the Array

The next pair of photomask designs is necessary to process the foundation for the array on the target substrate. The first design is used to recess certain regions of the target substrate, while the second photomask will allow for the bottom contact metallization. Both designs are very similar. The only difference is that the metal contact photomask is slightly smaller to make

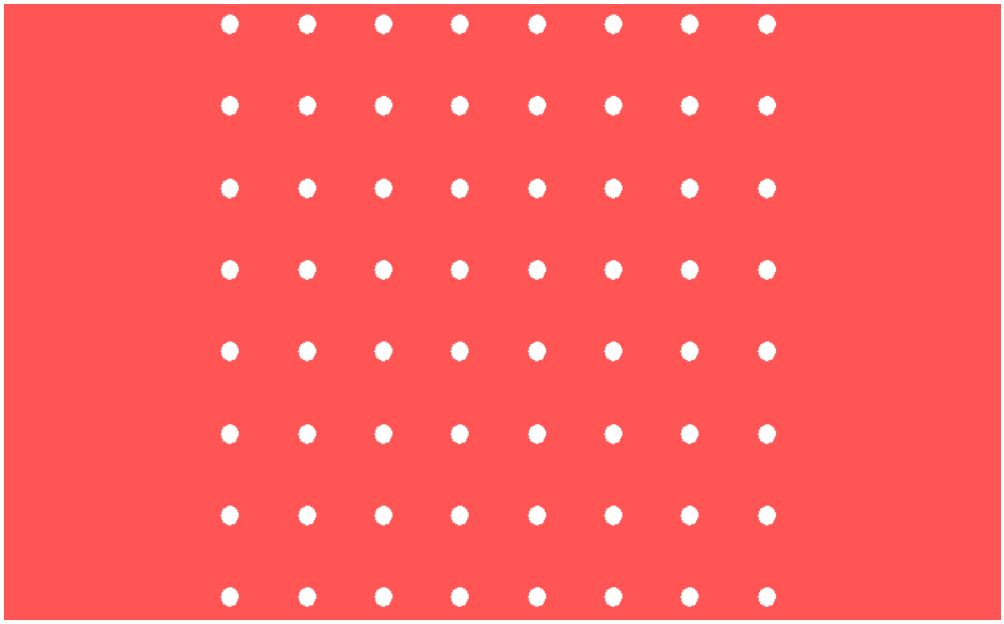

Figure 26 Photomask design for metallization of VCSELs.

certain that all the gold metal is inside the recess. Both designs consist of 25 arrays that include an 8 x 8 disk array with 8 horizontal lines running across them, with each line connected to two large contact pads, one at either end. For the recess photomask, the lines have a width of 12 μm and the disks have a diameter of 28 μm. The disks are 8 μm larger than the VCSEL diameter to allow for alignment tolerances (FCB) and higher probability of the VCSELs falling into the holes (FSA). The contact pads are 200 x 200 μm^2 and are designed for electrical probing of the array. For the metal contact photomask, the width of the lines is 10 μm and the diameter of the disks is 20 μm. The contact pad is 198 x 198 μm^2. Figure 27 shows the complete array and Figure 28 shows a close-up of one of the disk recesses. Figure 29 demonstrates how the metal (black) would fill in the recess.

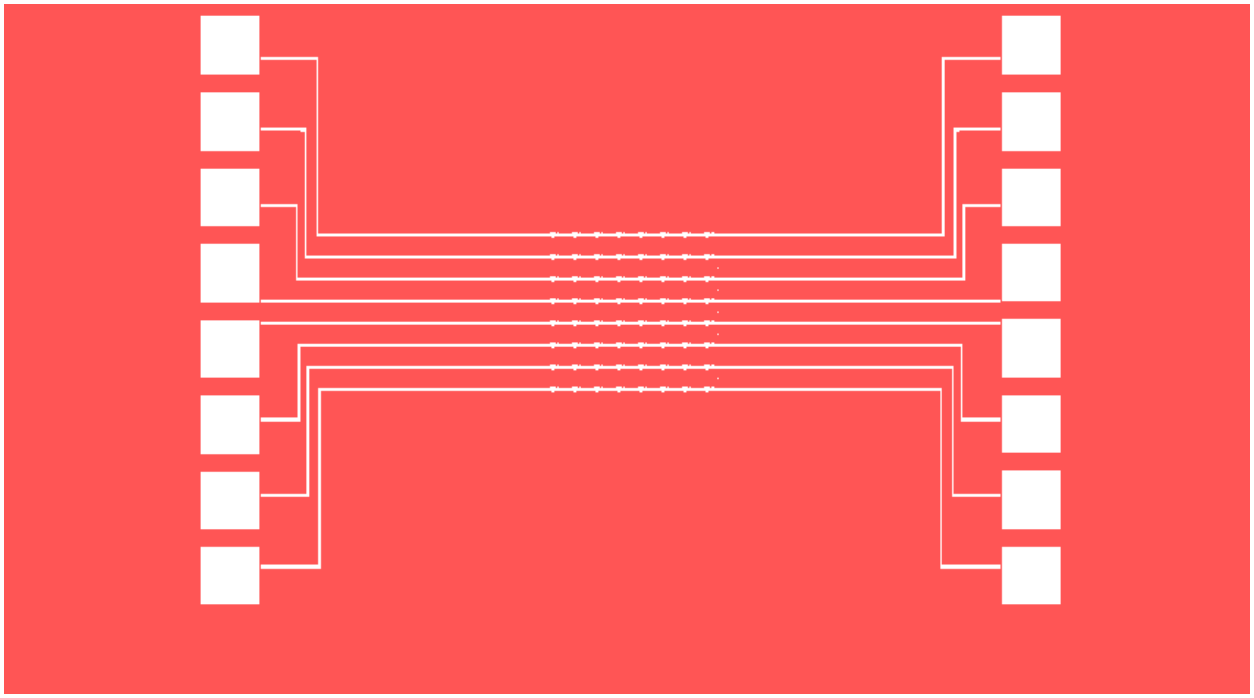

Figure 27 Etch design for one 8 x 8 array.

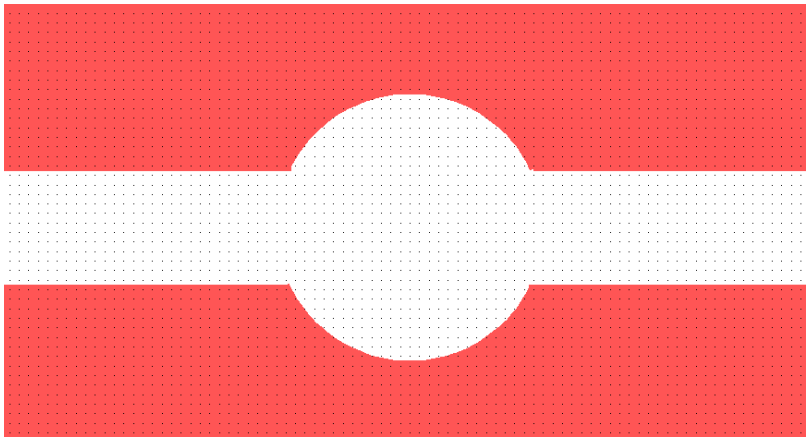

Figure 28 Close-up of disk in the etch design.

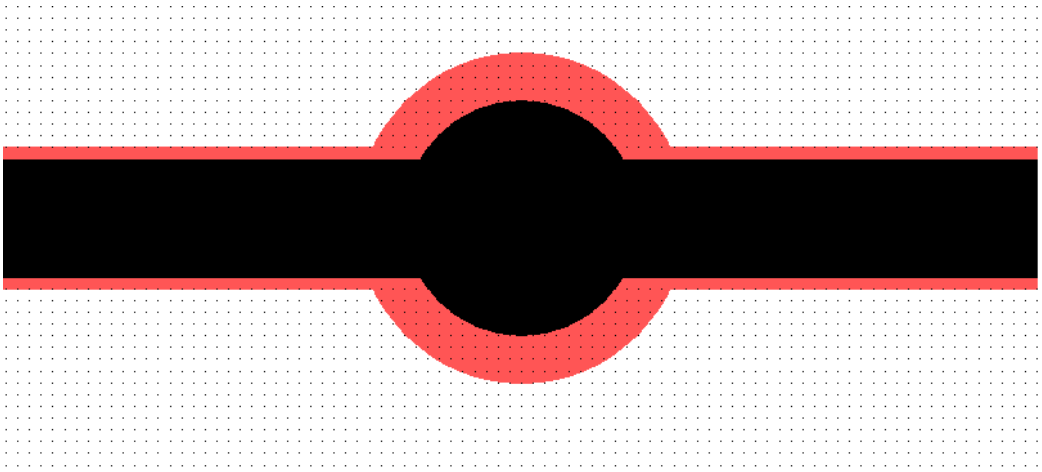

Figure 29 Demonstration of how metal fits in the recess.

3.8 Photomask Design for Etch Access Holes

With the FCB approach, the substrate with the VCSELs grown on them needs to be removed after the array has been bonded to the target substrate. This is accomplished by selectively etching the AlO lift-off layer. However, after the two wafers are bonded together, the etchant cannot get into the AlO layer. Etch access holes are necessary for the liquid to get into the AlO layer. For the design of this photomask, access holes need to be created in between the VCSELs, but I want to make sure that the etch does not destroy the VCSELs. The photomask design consists of square opaque blocks with circular holes. The blocks cover the 8 x 8 VCSEL array holes and the holes are situated away from the VCSELs. Figure 30 shows the design for the etch access photomask.

3.9 Photomask Design for Electrical Isolation

After the VCSELs have been transferred to the target substrate, there is the possible problem that the top metal contacts will short with the bottom metal contact. One potential solution to this problem is to place polyimide on the edges of the VCSELs and around the recessed hole to inhibit the top layer of gold from falling on the sides and to the bottom of the VCSEL. A ring

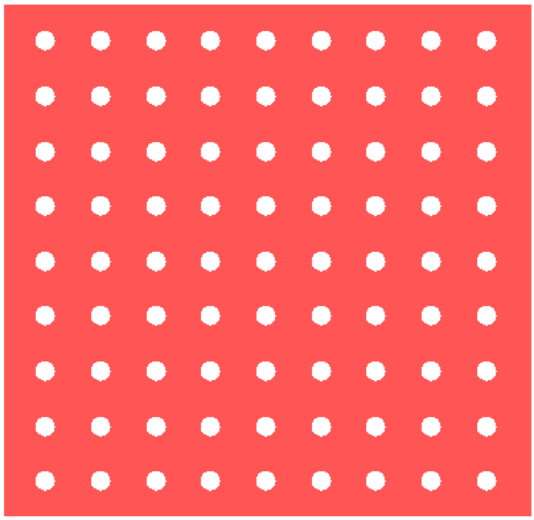

Figure 30 Etch access hole design.

photomask was designed to achieve this task. The ring has an outer diameter of 36 µm and an inner diameter of 18 µm. Figure 31 shows one of the rings.

3.10 Photomask Design for Top Layer Metallization

The last step is the top layer metallization. The top layer metallization is very similar to the bottom layer metallization. The main differences are that the top layer has the 8 µm aperture window to allow for the beam to propagate out and the metal lines run vertically instead of horizontally. The metal rings have a diameter of 18 µm and an inner diameter of 8 µm. A 2 µm cut is again used to help in the processing of the metal. Figure 32 shows one of the arrays for the top metallization. Figure 33 shows two of the ring contacts for the VCSELs.

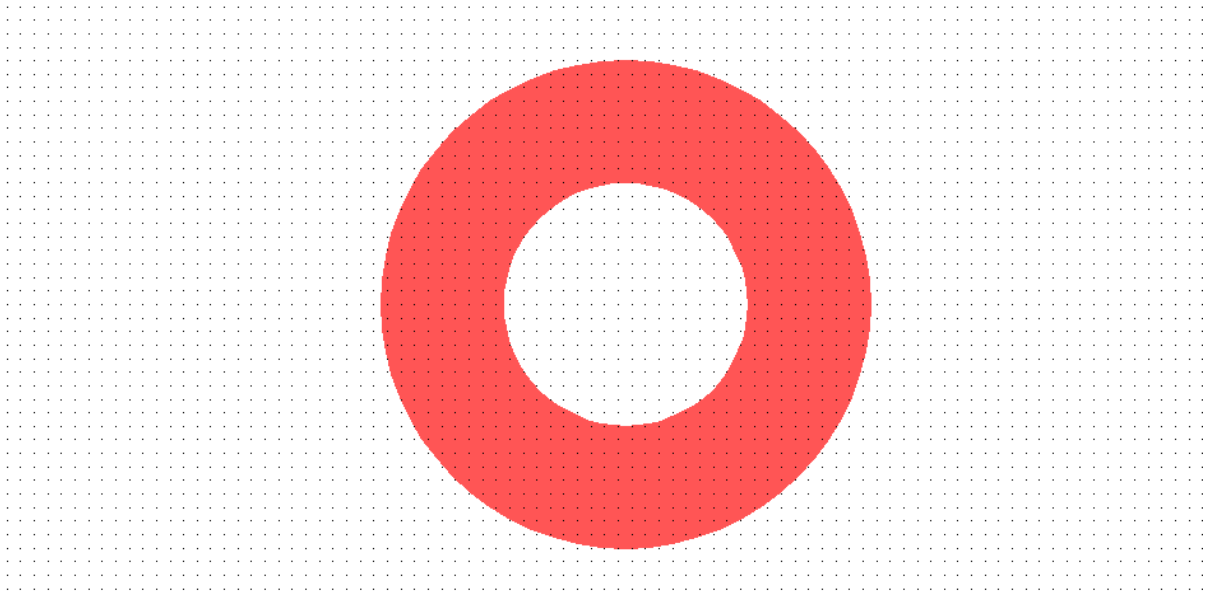

Figure 31 Layout of ring design used for the electrical isolation photomask.

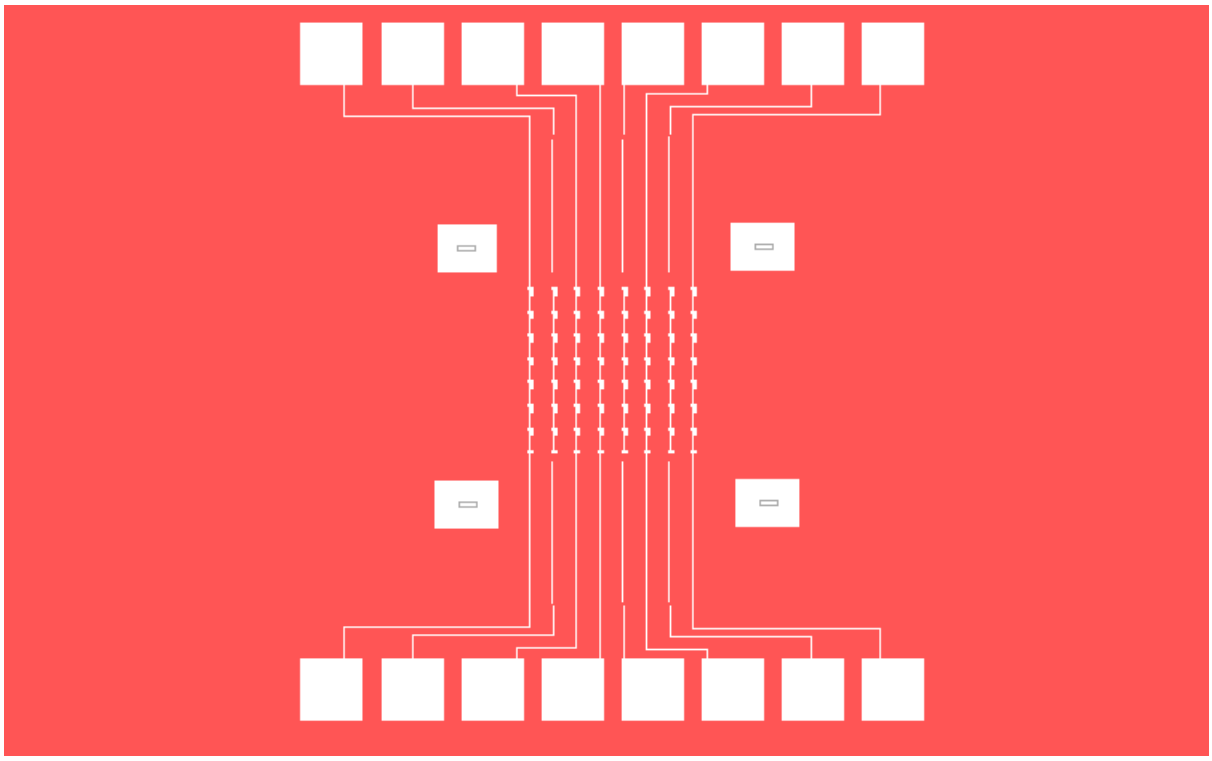

Figure 32 Design for top layer metallization.

Figure 33 Close-up of top metal contacts.

3.11 Self-Alignment Photomasks

One of the biggest problems with integrating the VCSELs onto another substrate is actually getting the VCSELs into the precise areas of the target wafer. One idea to accomplish this is to etch the array so that only the blocks with the VCSELs are left. Then on the target substrate a region that is slightly larger than the block can be etched so that the block will fit into the groove and no alignment will be necessary. Several designs are included in the photomasks to study this self-alignment process. 677 µm (approximate size of 8 x 8 array), 1000 µm, 2000 µm, and 4000 µm opaque blocks were created to etch the blocks. Figure 34 shows these blocks on the photomask. Clear block designs were created for the recess of the target wafer. The first set of blocks had sizes of 681 µm, 1004 µm, 2004 µm, and 4004 µm which gives a 4 µm tolerance and the other set of block have sizes of 685 µm, 1008 µm, 2008 µm, and 4008 µm which gives an 8 µm tolerance. Figure 35 shows a few of the clear blocks.

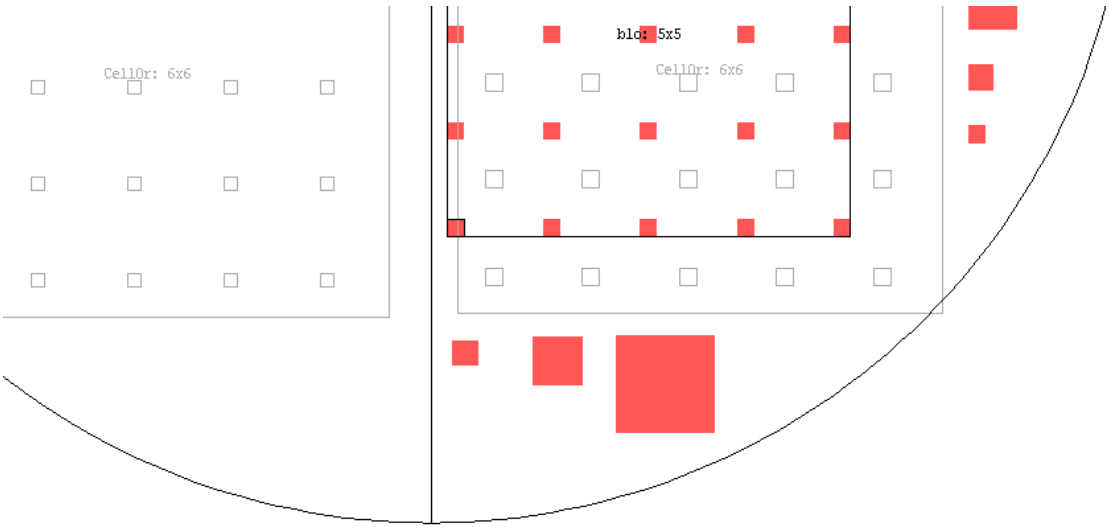

Figure 34 Block designs for self-alignment.

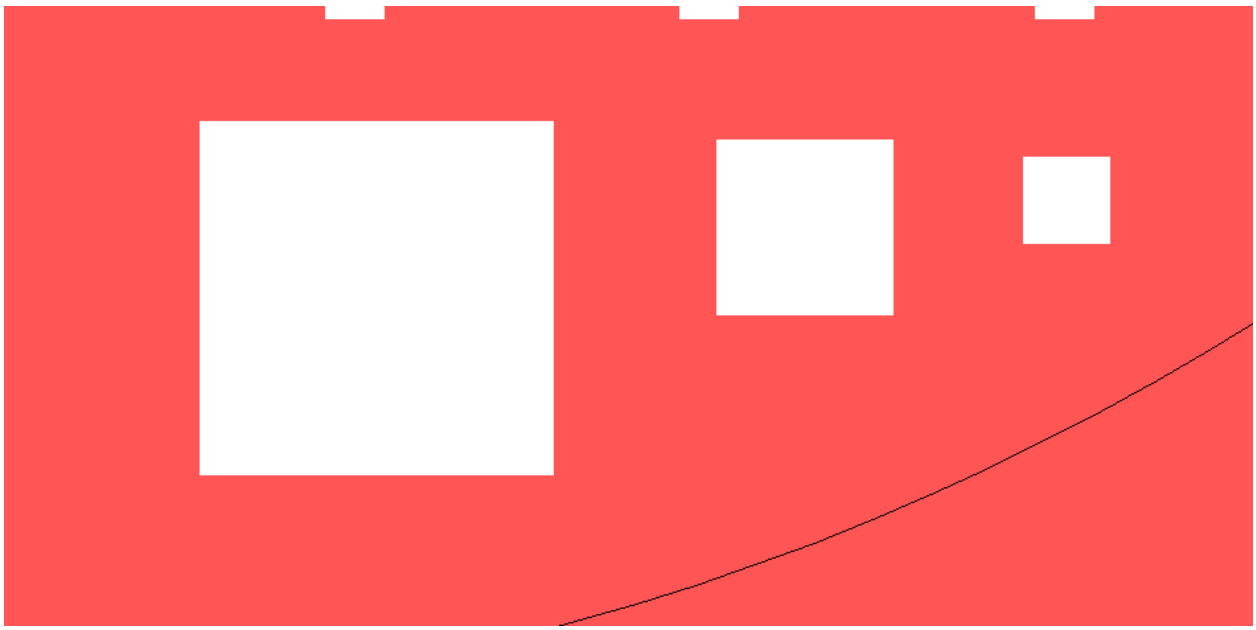

Figure 35 Block designs for recess in target substrate.

3.12 MUMPS® Design

A MUMPs® design was created so that the VCSELs could be integrated onto a MEMS substrate. Similar to the photomask designs for the host substrate, the MUMPs® layout contains holes for the VCSELs to be place in, a metal contact for each VCSEL with metal lines connecting rows of VCSELs, and bond pads to probe the devices. Figure 36 shows the complete layout of the MUMPs® design.

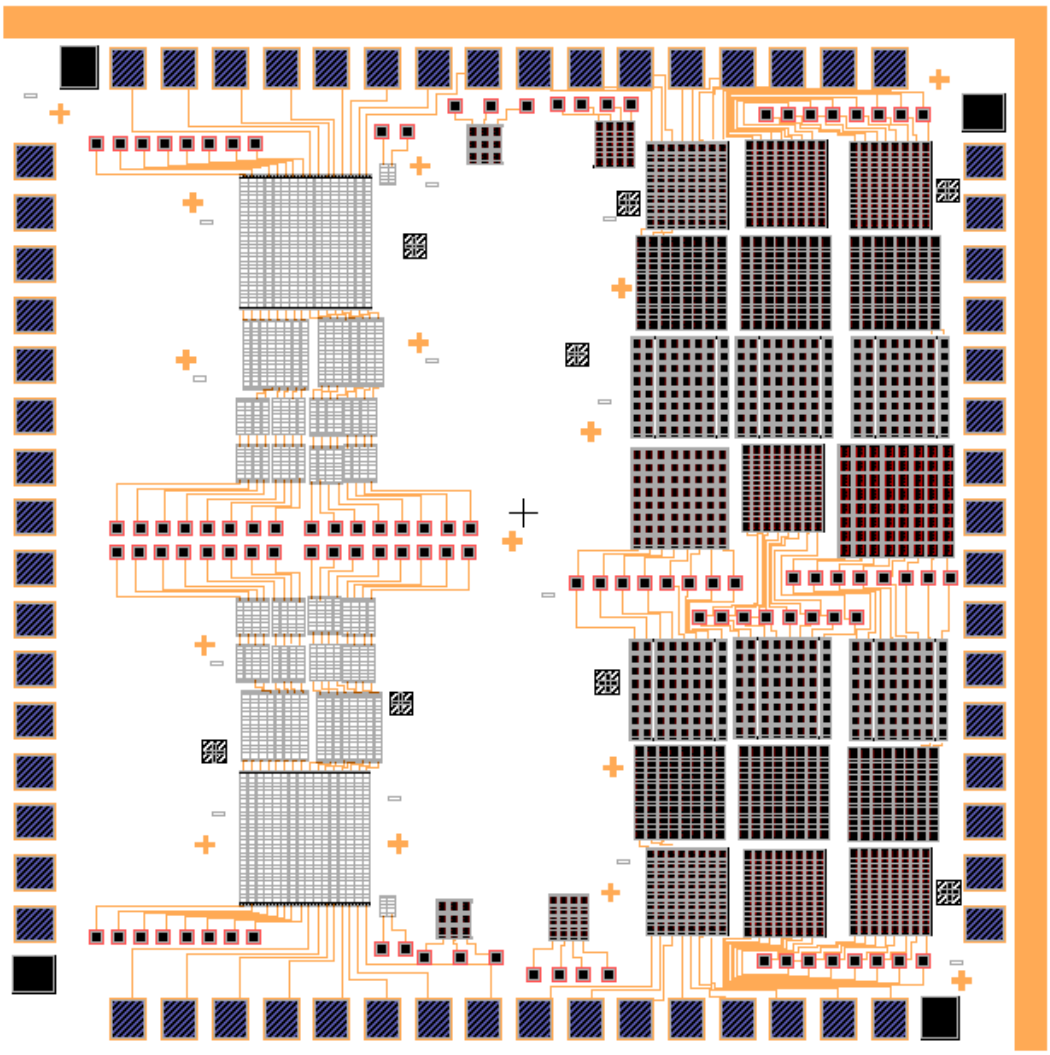

Figure 36 L-Edit layout of MUMPs® array design.

The MUMPs® process allows for holes to be created with varying depths. By removing polysilicon layers and trapping oxide, holes ranging from 0.5 µm to 6.75 µm can be created. Since metal contacts are needed in the hole and poly2 is required for the metal to bond to the wafer, the maximum depth of the hole is reduced to 4.75 µm. Figure 37 shows a cross-sectional view of the composition of the various depth holes that were designed. In addition to hole depth, the hole diameter and the array size were also varied in the designs. The diameter of the holes varied from 24 µm to 36 µm. Array sizes consisted of 16 x 16, 8 x 8, 4 x 4, and 3 x 3 holes.

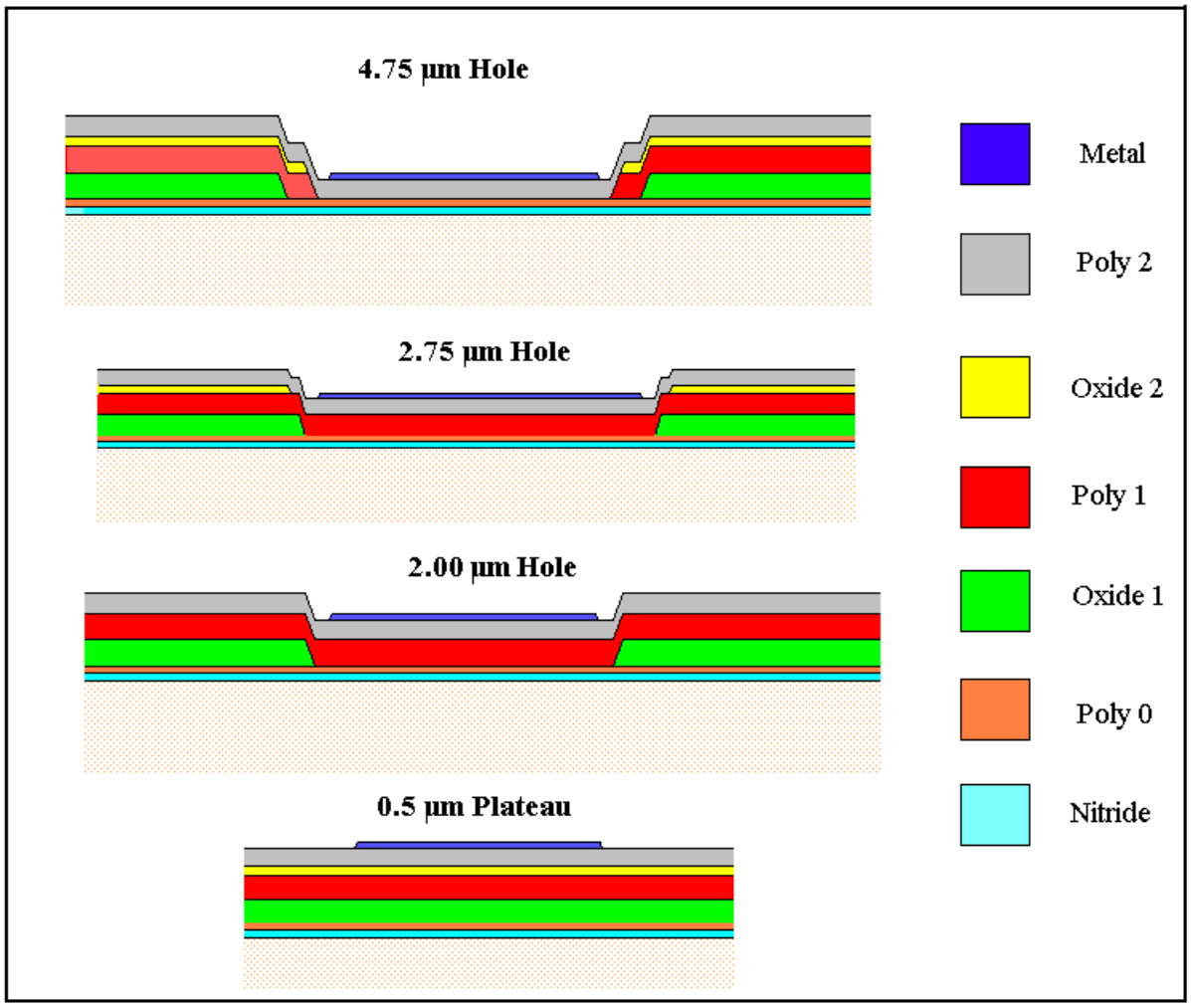

Figure 37 L-edit design of various hole depths that were included on the MUMPS® chip.

When designing each of the arrays, careful consideration of each design was required to ensure that each metal line was electrically isolated from the others and that the oxide was completely trapped. Each of the polysilicon layers that MUMPs® uses are conductive, however, the nitride layer is insulating. By eliminating all the polysilicon layers between the metal rows, electrical isolation between metal lines is achieved. Steps are also used in the designs to prevent any polysilicon from breaking off due to sharp drop-offs. The greatest drop in height in my designd is 2 μm. Figures 38 and 39 demonstrate the electrical isolation, oxide trapping, and the step drop-offs.

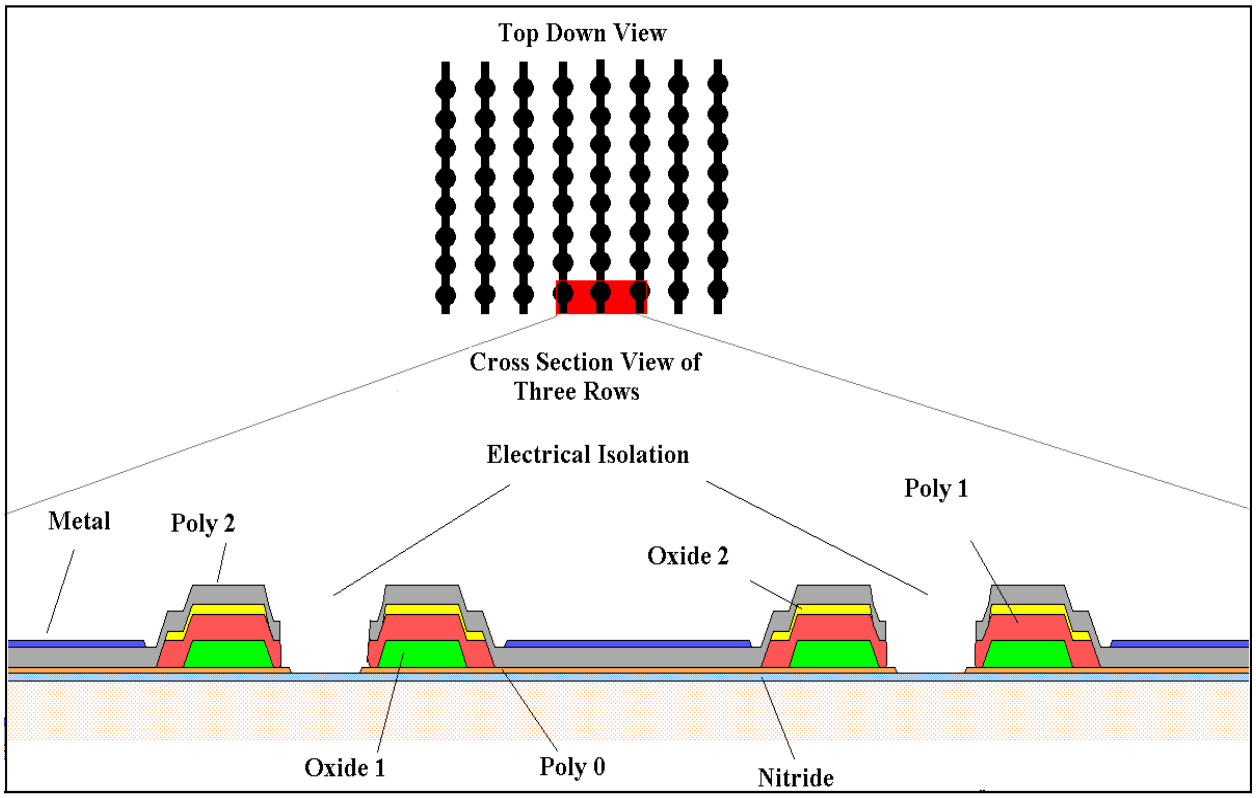

Figure 38 L-edit cross-sectional view of MUMPs® design illustrating electrical isolation.

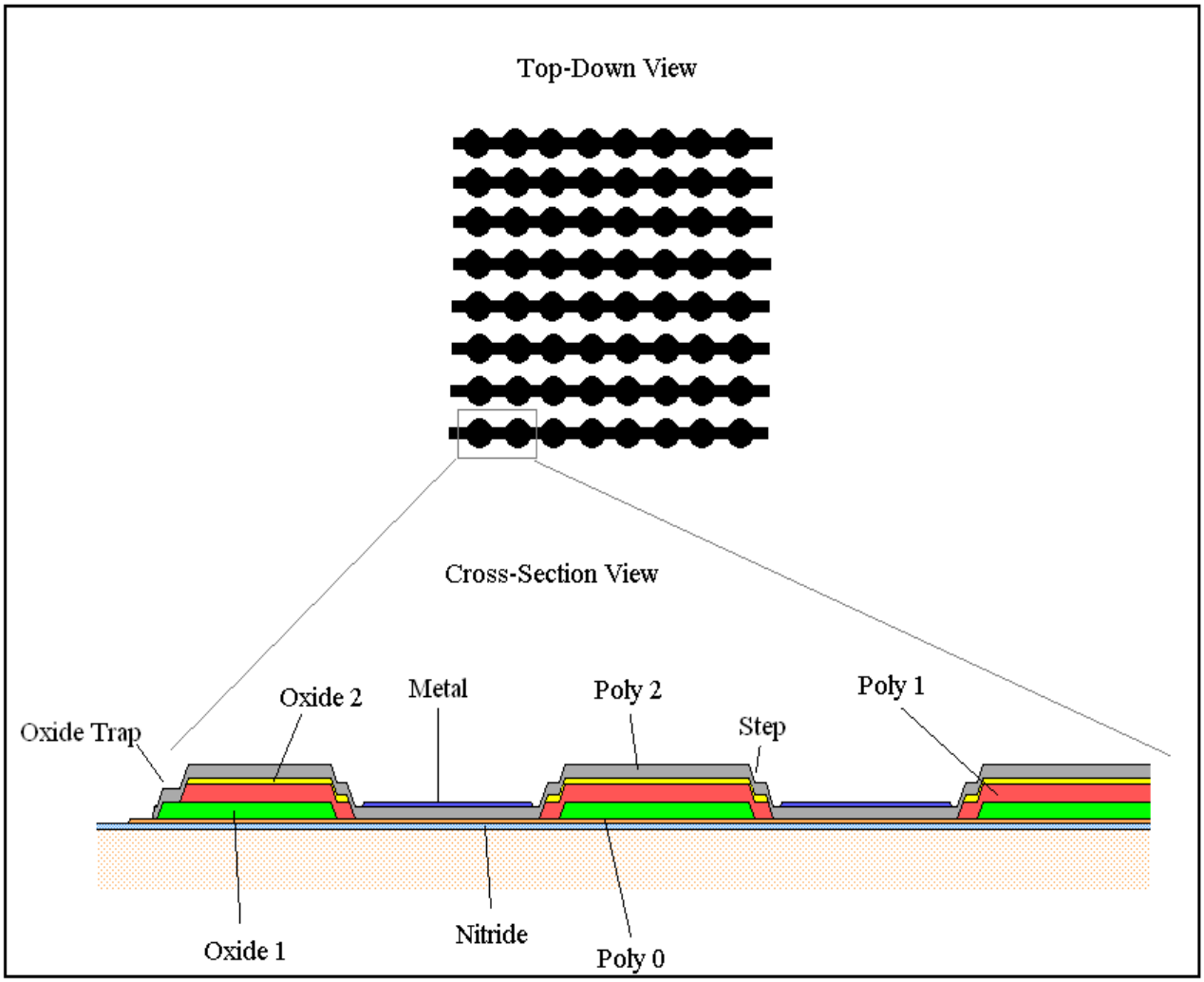

Figure 39 L-edit cross-section view of MUMPs® design demonstrating oxide trapping and step drop-offs.

3.13 Resistance Comparison of Matrix Array Designs

The design approach that I studied and developed for fabricating a matrix addressable VCSEL array has significant resistance benefits over the design described in Section 2.3.2. Instead of using an n^+ doped layer for one of the metal lines, I use a much less resistive material, gold, for my bottom line.

The resistivity of an n^+ doped material is given by:

$$\rho = \frac{1}{qn\mu_n} \qquad (\Omega/\text{cm}) \tag{3}$$

where ρ is the resistivity, n is the density of free electrons, q is the charge of the electron and μ_n is the electron mobility [1]. For a Si doping concentration of 10^{18} cm^{-3} in GaAs the resistivity is approximately equal to 10^{-4} Ω/cm [3]. The resistivity of gold is 2.35 x 10^{-6} Ω/cm, which is over 100 times less resistive. The total resistance of a material is given by:

$$R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right) \qquad (\Omega) \tag{4}$$

where R is the resistance, ρ is the resistivity, t is the thickness, w is the width, and l is the length [1]. For a width of 10 μm and a thickness of 0.2 μm, Figure 40 displays a plot of the total resistance of a gold line and a 10^{18} cm^{-3} Si doped GaAs as the length increases. Clearly the gold lines allow for much larger arrays to be fabricated.

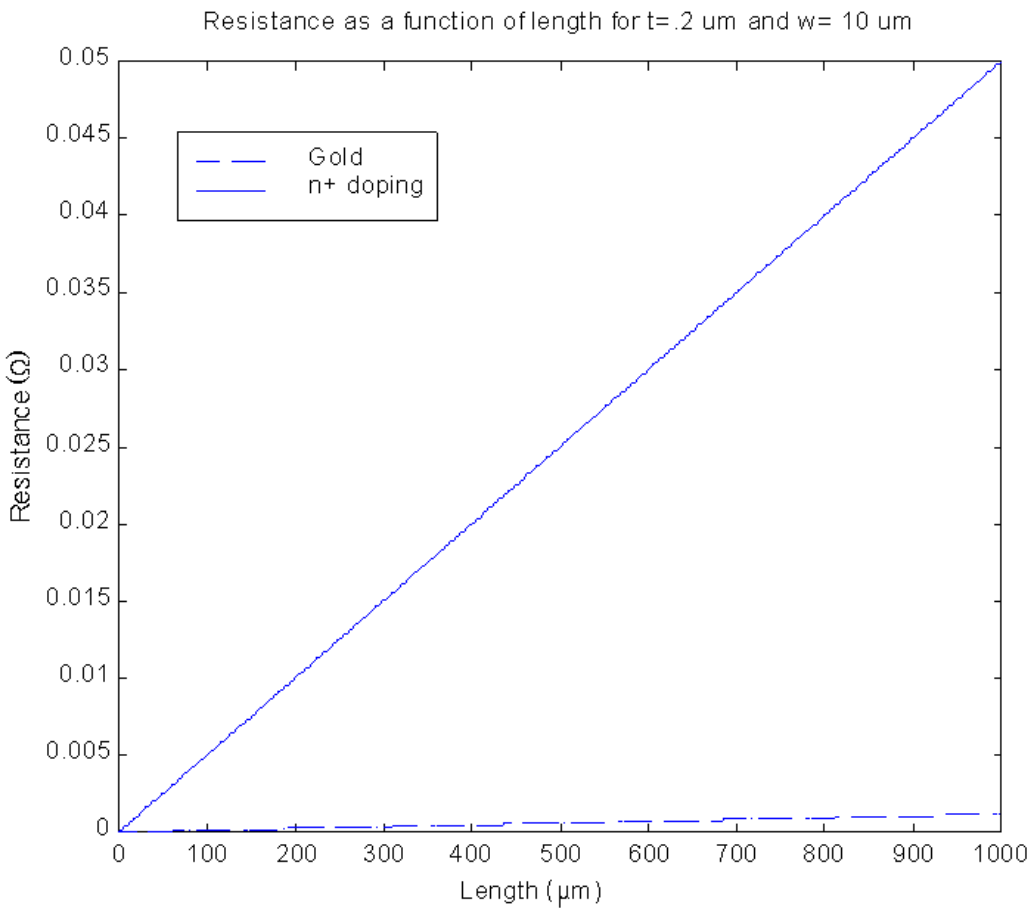

Figure 40 Plot of the total resistance of a gold line and a 10^{18} cm^{-3} Si doped GaAs line of width 10 μm and thickness of 0.2 μm, as the length is varied from 0 to 1000 μm

3.14 Summary

In this chapter, I presented the numerical modeling of a VCSEL structure. I also discussed the designs for the prototype photomasks that could be used to investigate the techniques required to fabricate an integrated VCSEL matrix addressable array. The twelve different designs have been laid out onto 3 photomasks. A MUMPs® layout containing various array structure is presented. The purpose of the design is to provide a recess for VCSELs and to contact the bottom of the VCSEL. Finally, I present results from a calculation and comparison of resistance for a metal line and an n^+ doped GaAs line

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2. "Photoplot Store", Contact Mr. Richard J. Sayer, 3355 N. Academy Blvd. #173, Colorado Springs, CO 80917-5103. Website, http://www.photoplotstore.com.

3. Sze, S. M., *Semiconductor Devices, Physics and Technology.* Murray Hill, N.J. 1985.

4. Experimental Processes and Equipment

4.1 Introduction

In this chapter, I discuss the equipment and processes that were used in my research for the fabrication of the matrix addressable arrays. I performed all of my processing steps in the AFIT cleanroom. Additional equipment was required to complete my experiments. Technicians at the Air Force Research Laboratory Sensors Directorate's cleanroom completed these additional processes. Photolithography, metal deposition, etching, and oxidation are the processing steps required to fabricate the VCSELs and the array.

4.2 Photolithography

Photolithography is a fundamental process for the fabrication of microelectronic devices. Photolithography involves the transfer of a pattern from a photomask onto a wafer. It entails the placement of photoresist over the wafer, the alignment of the mask with the wafer, the exposure of the wafer, and finally the development (removal) of the exposed photoresist. Through this process, designs with sub-micron features can be precisely defined onto a wafer.

4.2.1 Photoresist. The photolithography process first involves placing a light-sensitive material called photoresist over the entire surface of the substrate. When exposed to ultra-violet (UV) light, the chemical make-up of the photoresist is altered. Two different types of photoresist are available, positive photoresist and negative photoresist. For positive photoresist, UV light weakens the bonds of the photoresist. Developer will remove the weakened photoresist much faster than the remaining photoresist. Negative photoresist is the exact opposite. It will remain on the wafer after it is exposed to light and developed, while the developer removes the

unexposed photoresist [1]. Shipley series 1813 and 1805 positive photoresists are used in the photolithography processes for this thesis.

Photoresist is spun onto the wafer so that it coats the wafer as uniformly as possible. A few drops of photoresist are placed onto the middle of the wafer and the wafer is spun. The centripetal force of the spinning causes the photoresist to spread out over the wafer. As it spreads out, the photoresist coats the surface of the wafer and excess photoresist is spun-off. The recipe used for the photolithography processes are listed in Appendix A.

4.2.2 Alignment and Exposure. The mask aligner is a critical component of the photolithography process that serves two functions. First, the mask aligner aligns the wafer with the photomask. Secondly, it exposes the wafer and photomask with UV light. The Karl Suss MJB3 mask aligner, shown in Figure 41, located in the AFIT clean room was used for the alignment and exposure.

When the wafer is coated with the photoresist, there is a build-up of photoresist on the outside edges of the wafer, called edge bead. The edge bead can be quite substantial and keep the middle of the wafer from making contact with the mask or cause the photoresist to smudge the mask. Good contact with the photomask and wafer is necessary to prevent diffraction of the UV light that distorts the pattern. Therefore, removal of the edge bead is necessary to ensure precise and distinct designs.

While there are photomasks designed for edge bead removal, a piece of aluminum foil is a sufficient alternative. The aluminum foil is shaped and place on the wafer so that it covers the wafer except for the outside edges. The wafer is then loaded into the mask aligner and exposed. After all the edges have been exposed, the wafer is then placed into LDD26W developer for 30 seconds. After development, the outside edges of the wafer should be clean of photoresist.

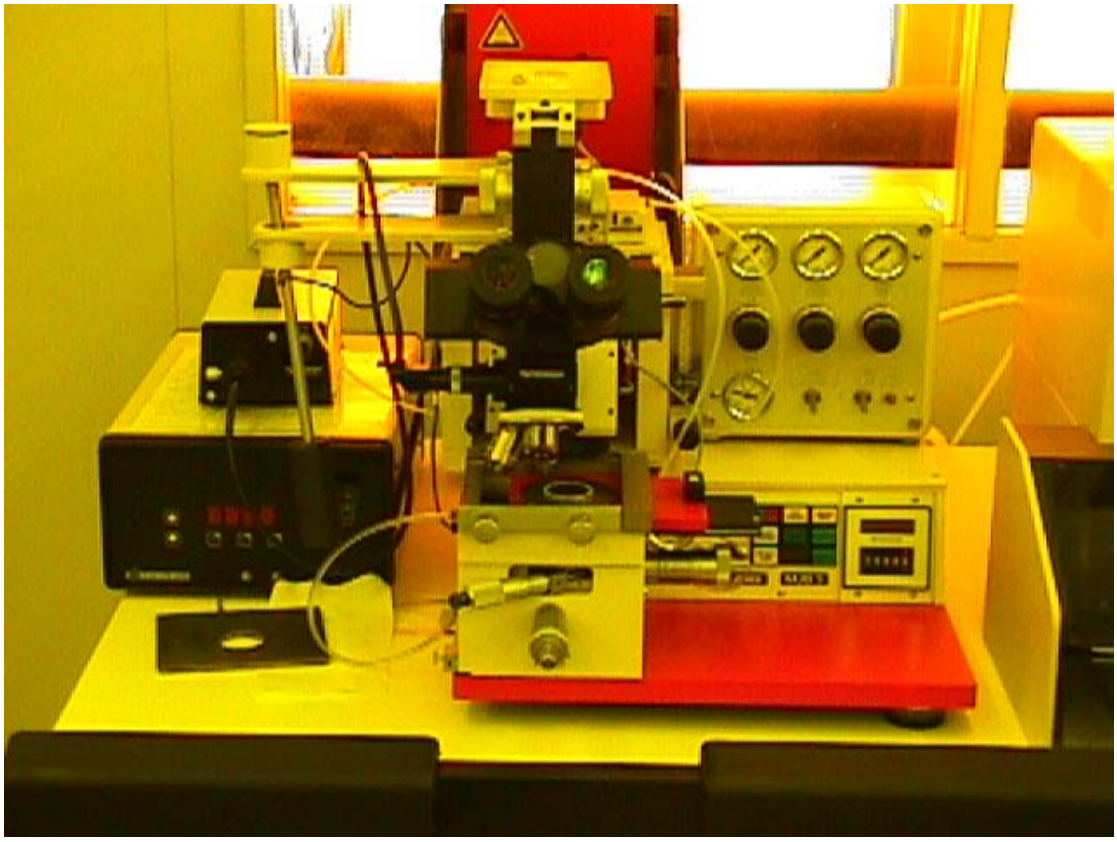

Figure 41 Karl Suss MJB3 Mask Aligner located in the AFIT cleanroom.

Except when alignment is not necessary, the next step is to align the wafer with the photomask. The photomask is placed onto a square metal plate with a circular hole in the middle. The plate is held by a vacuum so that the photomask cannot move. The plate is then placed under the microscope of the mask aligner. The user can move the wafer so that is in the correct position relative to the photomask. The mask aligner contains three knobs that allow for the movement of the wafer. The first two knobs control movement along the x-y axes while the third allows for rotational movement. Once the alignment has been completed the wafer is exposed to the UV light.

4.2.3 Development. After the wafer has been exposed to the UV light, the photoresist must be developed so that the exposed photoresist can be removed from the wafer. The wafer is

placed into a solution of deionized water and 351 developer in a 5:1 volume ratio. The wafer is then inspected under a microscope to assure that the wafer has been fully developed and that the designs have been transferred to the wafer successfully.

4.3 Electron Beam Metallization

To provide the electrical contacts necessary for the VCSELs and to bond the VCSELs to a different substrate, metal had to be deposited on the wafer. Metal deposition was accomplished through the use of the electron beam evaporator. The electron beam evaporator uses an electron beam to change solid metal into a gaseous vapor. The gaseous vapor is directed toward the sample and coats the surface of the sample. The electron beam evaporation is a quick process that has low contamination. Figure 42 shows the electron beam evaporator.

For this thesis two different metal depositions were required. The VCSEL devices require both an n-contact and a p-contact, with different metal compositions necessary for each type. For the n-contact, metal was laid down in the following order; 170 Å germanium, followed by 330 Å gold, 250 Å nickel and 2000 Å gold. The p-contact consisted of 500 Å titanium followed by 1500 Å of gold.

4.4 Etching

Etching is a process where material is removed from the wafer. There are two different types of etchants, wet and dry, as well as two types of etches, anisotropic and isotropic. In the anisotropic etch, material is removed from the substrate much faster in one direction than another. Anisotropic etches allow straight sidewall and flat surfaces to be created. Isotropic etches etch uniformly in all directions and typically form structures with rounded features [2].

Figure 42 Electron beam evaporator located in the AFIT cleanroom.

Figure 43 contrasts the two types of etches. Dry etches are typically anisotropic, while wet etches can be either isotropic or anisotropic. Etching is performed to create a trench for the bottom layer metallization and for the VCSEL to lie in. Etching is also used to form the VCSEL mesas.

4.4.1 Reactive Ion Etching. Reactive ion etching (RIE) is an anisotropic dry etch that achieves high aspect ratios in most cases perpendicular to the wafer [2]. Radio frequency (RF) power drives the chemical reactions that result in the etching of the wafer [2]. RF energy accelerates electrons giving them enough kinetic energy so that when they collide with the low pressure gas that is in the chamber they break the chemical bonds of the gas and create ions

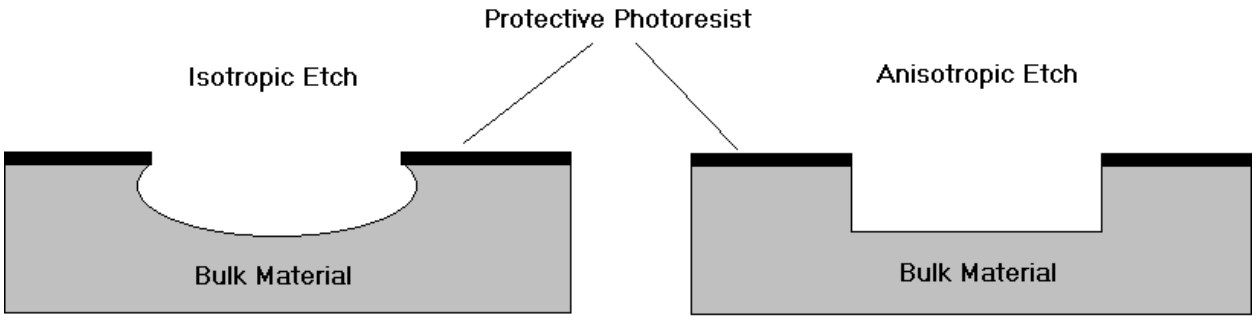

Figure 43 Illustration of an isotropic and an anisotropic etch.

and more electrons. The ions are accelerated and bombard the surface of the wafer. The bombardment causes etching of the wafer normal to the direction of the wafer [5]. Figure 44 shows an RIE system. The RIE etch is required to create the VCSEL mesas and to provide a recess for the VCSELs and bottom layer metallization on the target wafer.

4.4.2 Sulfuric Acid Etch. A sulfuric acid solution provides a wet isotropic etch that is simple to perform. The etchant is a solution of hydrogen peroxide, sulfuric acid, and deionized water in a 1:1:10 volume ratio. The solution should be allowed to cool down for several hours in order to obtain a more predictable etch rate since mixing the chemicals causes the solution to heat up. The solution etches at an approximate rate of 100 Å/sec. However, an etch rate study should be done prior to the actual etching of the sample to obtain a more precise etch rate. The sulfuric acid etch does not allow for straight sidewalls like the RIE but is simple and does not require any equipment.

Figure 44 Phantom RIE system [5].

4.5 Scanning Electron Microscope

Conventional microscopes that are located in the AFIT cleanroom offer a limited magnification of 50x and can only offer a top down view. To determine the success or failure of different processes greater magnification or an angled view is necessary. The scanning electron microscope (SEM) offers these capabilities.

The SEM is a microscope that uses electrons rather than light to form an image. There are many advantages to using the SEM instead of a light microscope. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at one time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of the samples is relatively easy since most SEMs only require the sample to be conductive [3].

The SEM works by producing a beam of electrons at the top of the microscope by heating a metallic filament. The electron beam follows a vertical path through the column of the microscope. It makes its way through electromagnetic lenses, which focus and direct the beam down towards the sample. Once it hits the sample, electrons are ejected from the sample. Detectors collect these secondary or backscattered electrons, and convert them to a signal that is sent to a viewing screen forming a picture [3]. Figure 45 shows a picture of AFIT's SEM.

Figure 45 Scanning Electron Microscope located in the AFIT test room.

4.6 Profilometer

It is often advantageous to know the thickness variations on the surface of the wafer. The profilometer is a machine that is capable of detecting small vertical variations on the surface of a wafer. Whether the user wants to know the thickness of a deposited material or if he/she wants to know the variation in the surface of the wafer, the profilometer can determine the step height with a vertical resolution of 5 angstroms [4].

The profilometer measures the height difference using a stylus. The stylus is a thin needle with a tip radius of 12.5 μm [4]. The stylus is lowered onto the surface of the wafer and scans across a small region of the wafer. The stylus measures the surface variation and then sends the data to the computer in the form of a vertical variation vs. horizontal distance plot. I used the Tencor Alpha Step 200 Profilometer shown in Figure 46 to determine photoresist thickness, metal deposition, and etch depth.

Figure 46 Tencor Alpha Step 200 Profilometer located in the AFIT cleanroom.

4.7 Summary

In this chapter, I explained the procedures and equipment necessary to fabricate a VCSEL matrix addressable array integrated onto another substrate through FSA and FCB techniques. In Chapter 5, I will analyze the results obtained through the use of this equipment.

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3. Material Science and Engineering Department at Iowa State University "Welcome to the World of Scanning Electron Microscopy", http://mse.iastate.edu/microscopy/home.html. information taken from internet in January 2002.

4. Microelectronics Research at the University of South Florida Home Page. http://cmr.eng.usf.edu/cleanroom/tools/alpha_step.html. Information taken from internet in January, 2002.

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5. Results and Analysis

5.1 Introduction

In this chapter, I will discuss the results of my experiments. I begin by discussing the results of my VCSEL fabrication. I will then show the MUMPs® chip that was fabricated to be used as the target substrate. Finally, I will discuss the experiments that were performed to fabricate arrays.

5.2 VCSEL Fabrication

In my initial experiments, I wanted to study and develop a process for the lift-off of the VCSELs and transfer them onto another substrate. I needed to demonstrate that the VCSELs worked before lift-off. Once that was demonstrated, I would focus on getting the VCSELs lifted off for each approach (FCB and FSA) and randomly place them on the target wafer. Finally, I wanted to place the VCSELs in precise positions on the target wafer.

5.2.1 FSA VCSELs. The process for testing the VCSELs is to use the ring photomask to deposit metal rings onto the material, etch the VCSEL mesas, oxidize, and backside metallize the wafer. Once the VCSELs have been tested, they could be lifted-off and those that landed with the ring side-up could be tested again to see if they would still work.

I originally had difficulties with the photolithography of the rings resulting from the extreme size of the device, only 4 μm in width. After adjusting my exposure and development times, I was able to get the rings to develop through. I was then able to deposit metal (500 Å Ti followed by 2000 Å gold) on a few samples. However, when I performed the metal lift-off all of the gold peeled off. The bottom metal layer, titanium, was still visible on the wafer (Figure 47), which

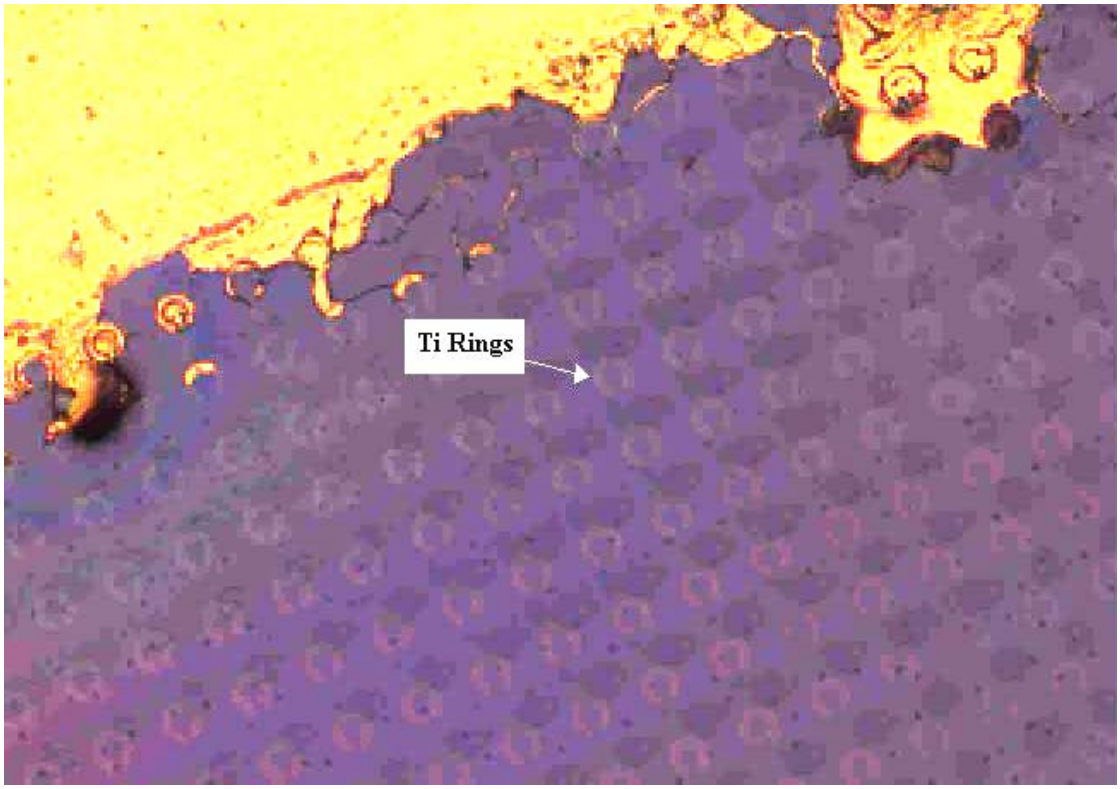

Figure 47 Microscope image (10x) of VCSEL wafer with Ti rings remaining on wafer after metal lift-off. Gold rings should be on top of the Ti rings.

demonstrates that the photoresist was completely removed from those areas of the wafer. I then concluded that the gold was not breaking off onto the wafer, instead it remained a continuous sheet. After talking to some other researchers, I adopted an alternative metal deposition process (Appendix B). By spinning on XPLOR 4A before the photoresist, the problem of the gold being a single sheet across the entire wafer is avoided. When the exposed photoresist is developed, it undercuts the underlying XPLOR 4A making the gold break from the photoresist to the wafer as demonstrated in Figure 48b. When using the XPLOR 4A, I was able to get the metallization to lift-off correctly. The metallized wafer is shown in Figures 49 and 50. The next step required is an RIE etch, however, the equipment was unavailable when I needed it.

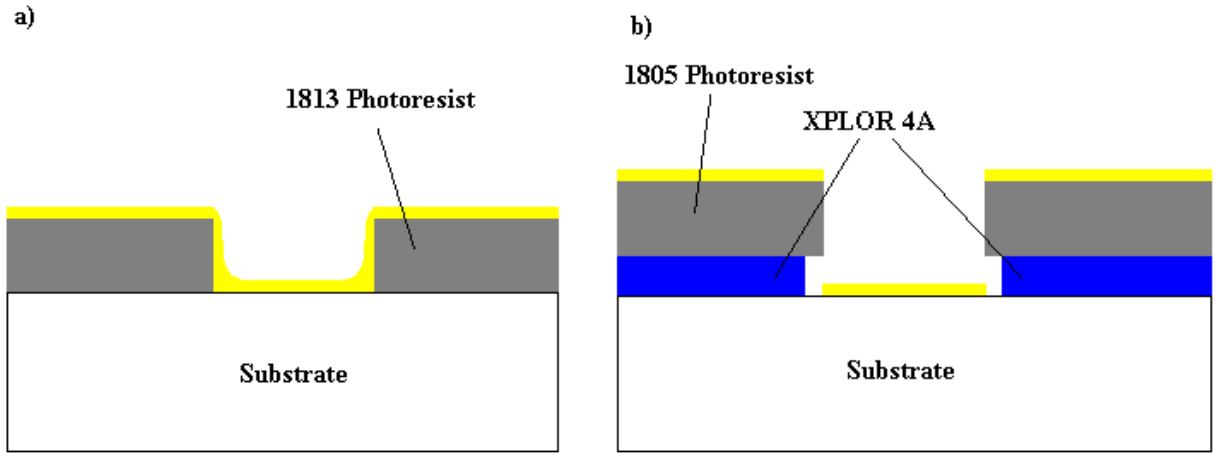

Figure 48 Illustration of a) possible problem of continuous gold coating and b) how undercutting of XPLOR 4A can alleviate this problem.

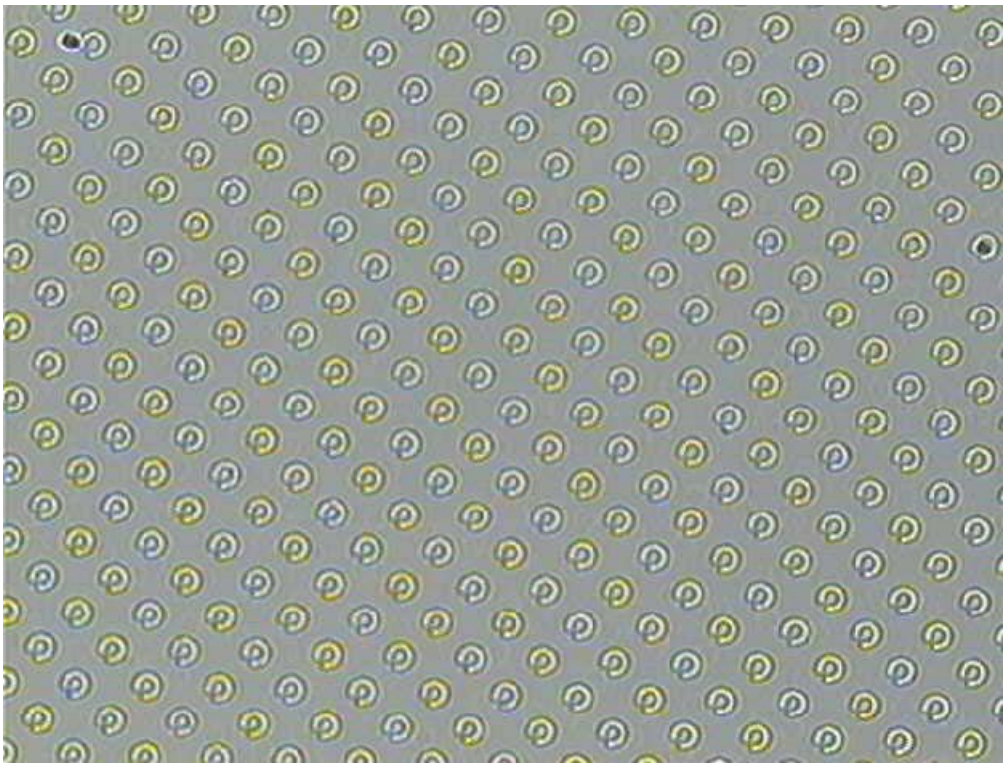

Figure 49 A microscope image (4x) of the metallized rings.

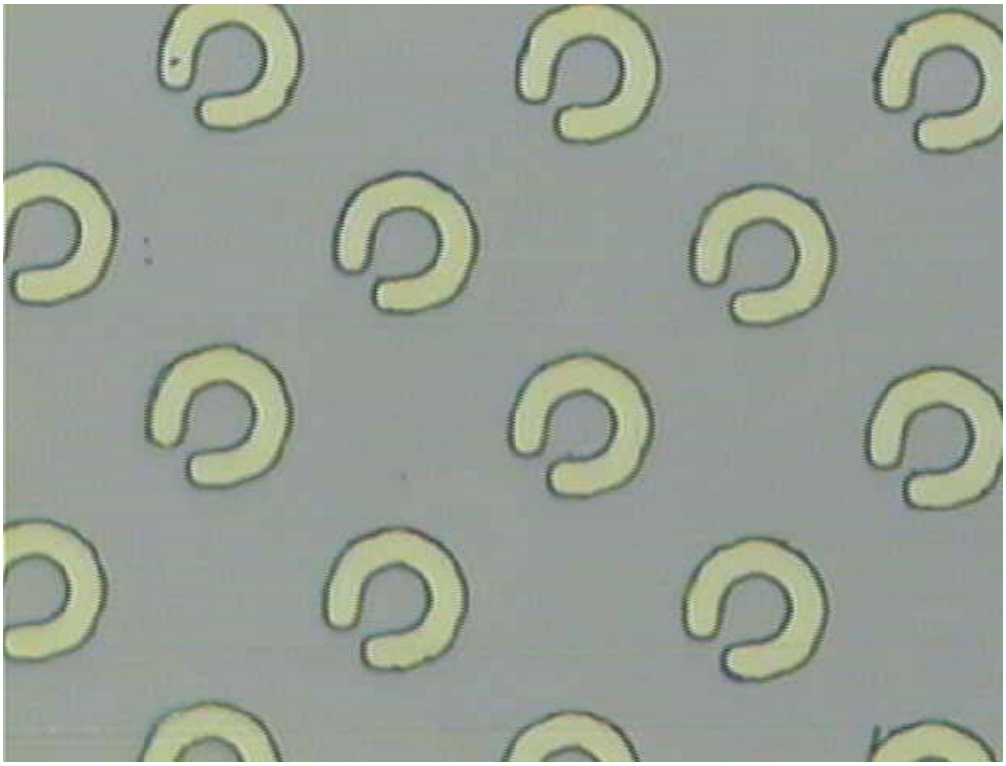

Figure 50 Microscope image (20x) of metallized rings.

5.2.2 FCB VCSELs. The VCSELs designed for FCB integration cannot be tested on wafer because they need to be bottom-emitting on the host wafer. When they are flipped over onto the target wafer they will emit away from the surface of the wafer. The first process is then to place solid metal circles onto the wafer. The metal will enable the bonding of the device to the target wafer and also serve as the n-contact. Metal was deposited to form the 8 x 8 circle array. Figures 51 and 52 show microscope images of the gold.

After the metal deposition, photoresist was again patterned over the gold circles to protect them during the etch. The masks were designed assuming that an RIE etch could be performed to create straight sidewalls. However, the RIE was either reported to be having problems or unavailable when I needed it. Consequently, a wet etch was performed to create the mesas. Sulfuric acid was used to etch down 8 μm. The problem with the wet etch is that it erodes the

wafer in all directions. The metal circles are only 20 μm in diameter while a 7.75 μm etch is required to etch down to the lift-off layer. For a truly isotropic etch, this would thin the VCSELs down to 4 μm in diameter. A quick look under the microscope verified the problems. Figure 53 shows that the gold rings have come off of the wafer. Figures 54 and 55 show SEM photos of the mesas and how the etch eroded the structures.

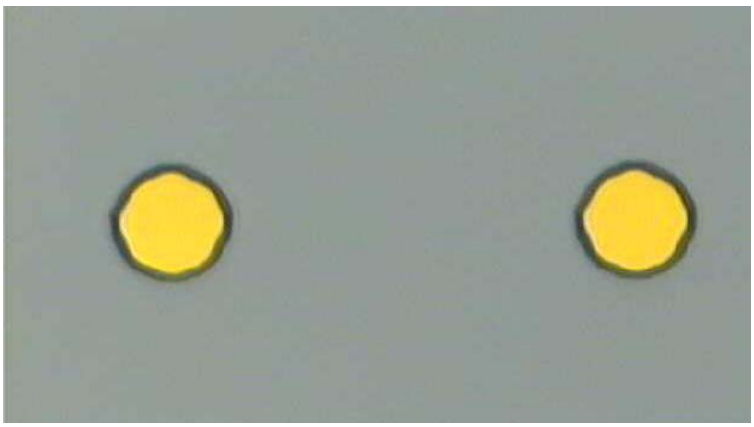

Figure 51 Microscope image (50x) showing gold circles.

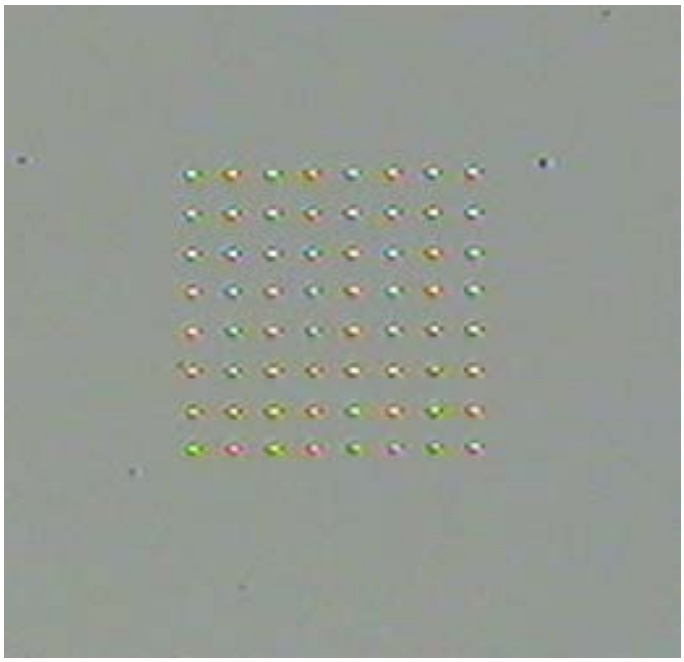

Figure 52 Microscope image (50x) of the metallized array.

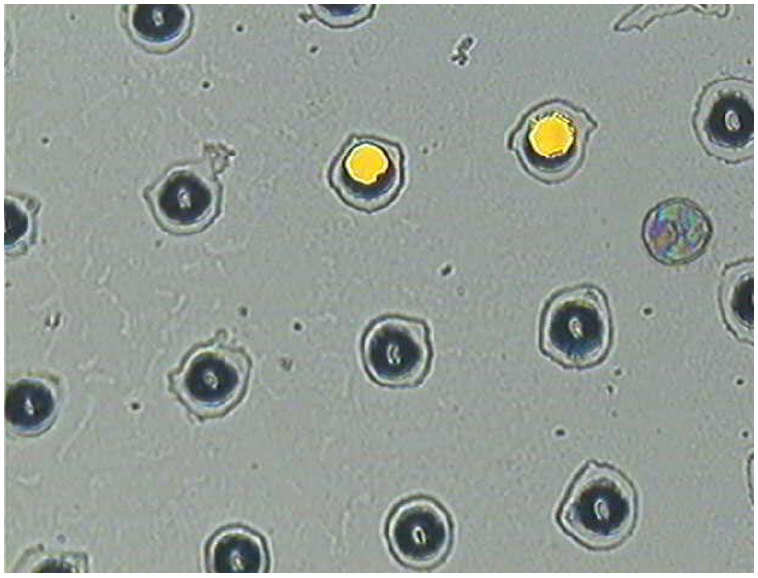

Figure 53 Microscope image (30x) of array after wet etch was performed. These two gold rings were the only ones remaining on the entire wafer.

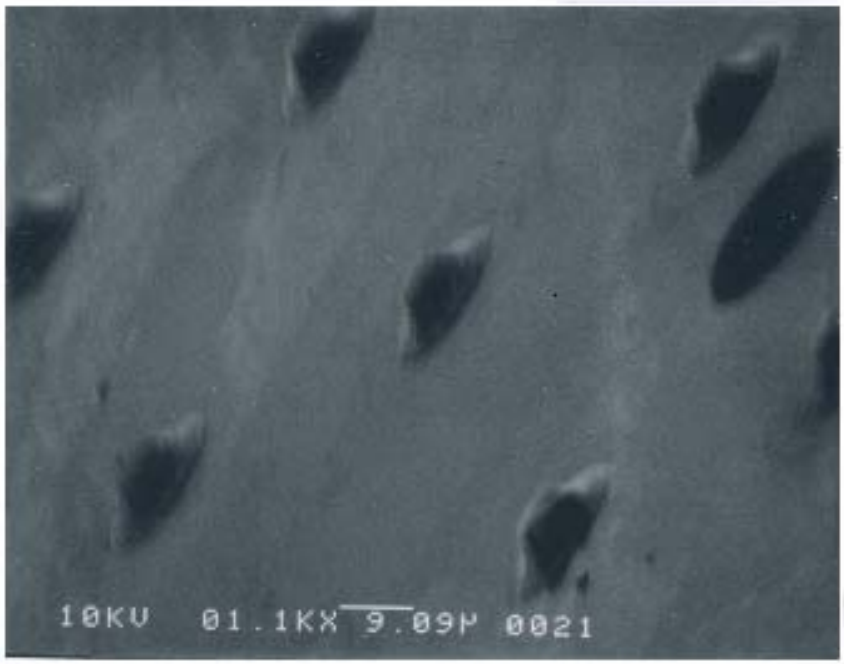

Figure 54 SEM photo (1100x) of mesas after wet etch was performed. Picture clearly shows that the sulfuric acid etched far into the sides of the device.

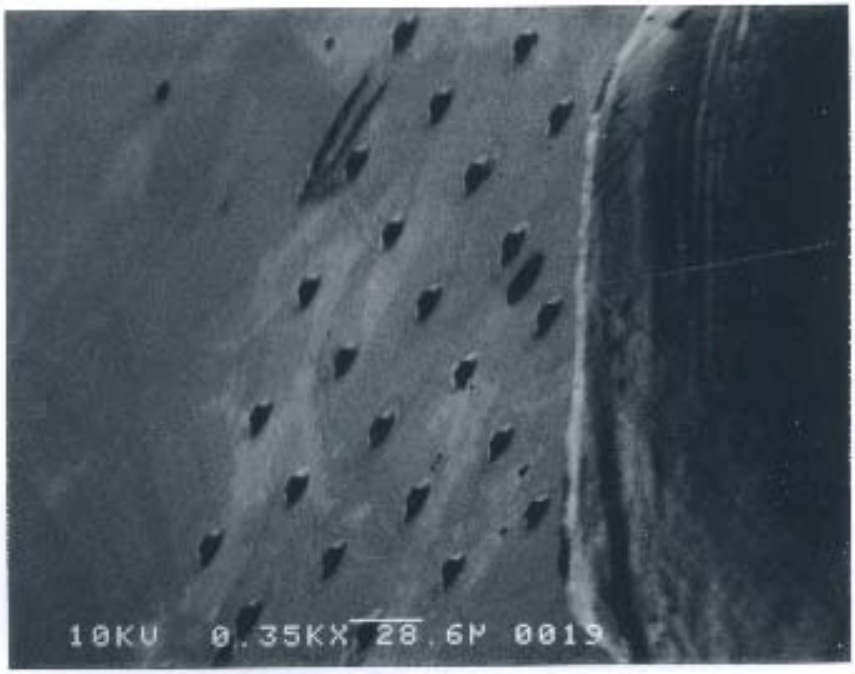

Figure 55 SEM photo (350x) of mesas after wet etch.

5.3 MUMPs® Chip

A chip was fabricated using the MUMPs® process. Sixteen quarter die (0.25 cm^2) all with the same design were fabricated. Figure 56 shows a portion of the die and Figure 57 shows one of the 8 x 8 arrays. The varying designs allow for FSA and FCB techniques to be used and tested for the best configuration to integrate devices into the holes. Figure 58 shows two of the designs with different size holes. The chip functions as the bottom metallization layer for a matrix addressable array. Metal lines interconnect between arrays to conserve bond pads on the chip and large portions of the chip were left vacant to allow for the top metallization bond pads to be placed. Figure 59 shows some of the metal wiring between bond pads and arrays. One of the main benefits of using the MUMPs® process is that they allow for electrical isolation on the die. Figure 60 shows the isolation between rows to prevent cross-talk between active lines.

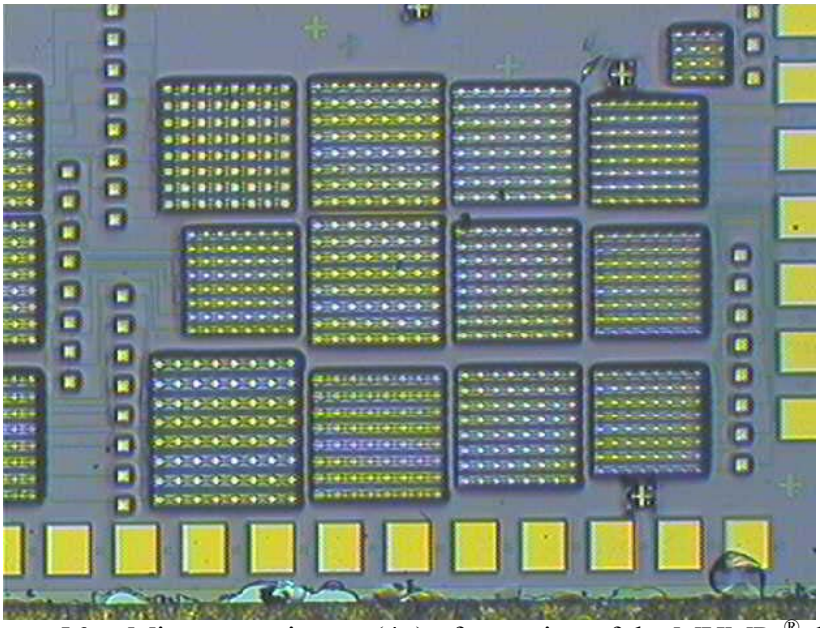

Figure 56 Microscope image (4x) of a portion of the MUMPs® die.

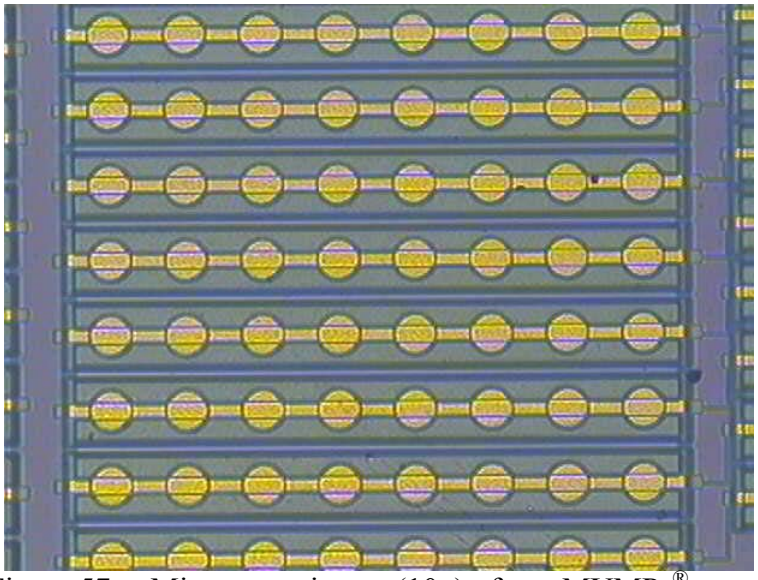

Figure 57 Microscope image (10x) of one MUMPs® array.

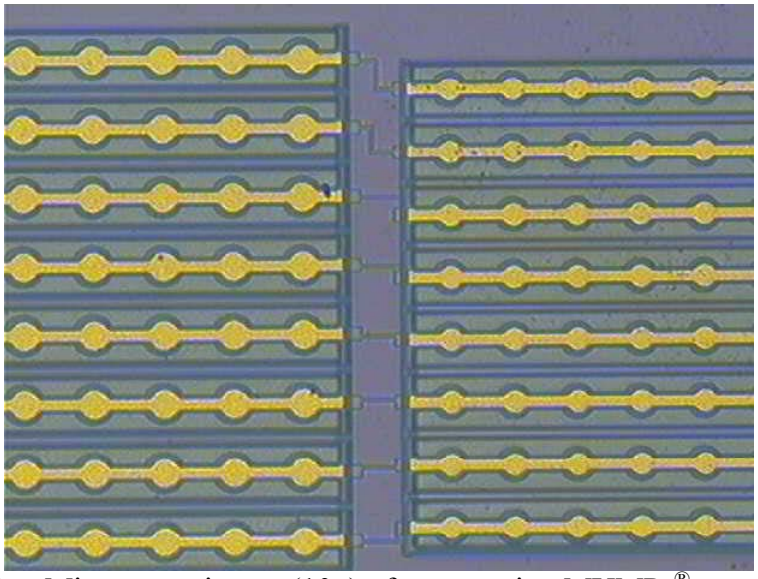

Figure 58 Microscope image (10x) of two varying MUMPs® array designs.

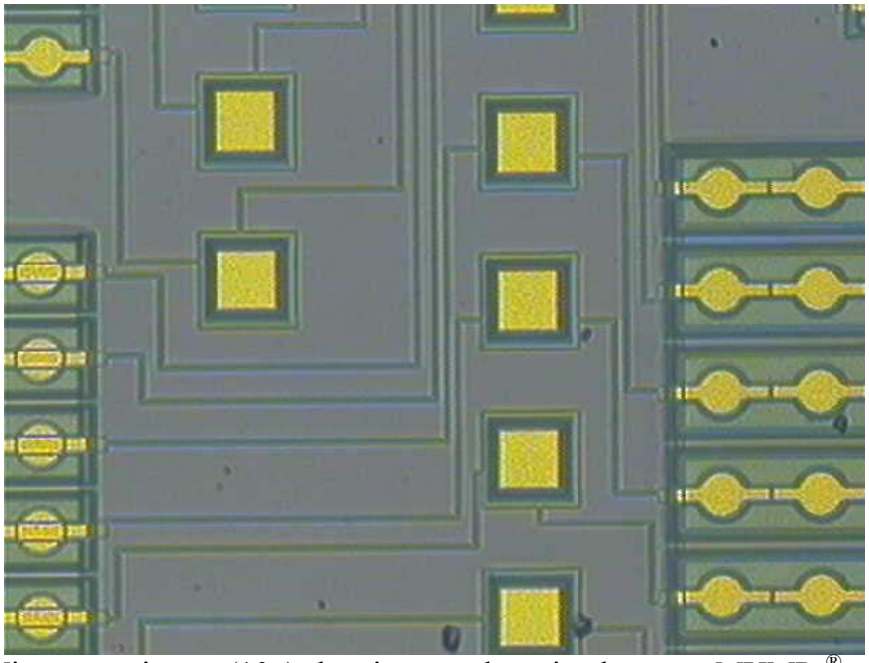

Figure 59 Microscope image (10x) showing metal routing between MUMPs® arrays and bond pads.

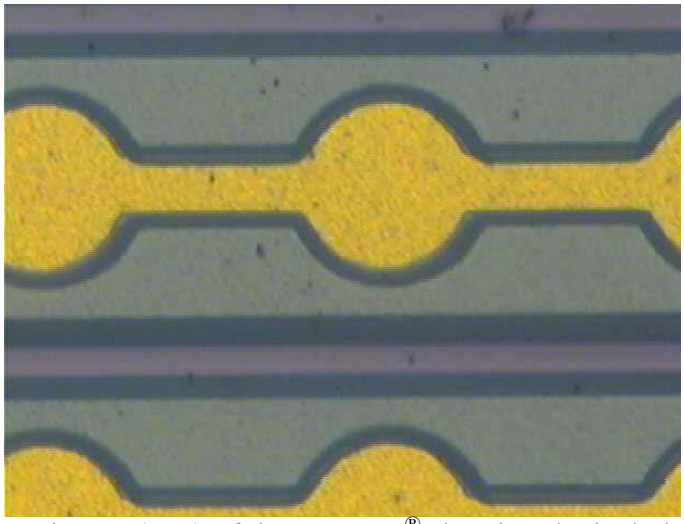

Figure 60 Microscope image (50x) of the MUMPs® showing the isolation between adjacent rows.

5.4 Matrix Array

The matrix array consists of the bottom layer metallization, an insulating layer, and the top layer metallization. The first concern that had to be addressed was that the top layer metallization must be within a few tenths of a micrometer height difference with the top of the VCSEL to assure that the metal lines will not break. Three different methods were studied as possible solutions each containing their own difficulties.

5.4.1 Recess Study. The first study was to recess the substrate to a height equivalent to the VCSEL. The device I was working with is about 7.7 μm high. Using the sulfuric acid, I etched a trench for the metal 7.9 μm deep. I then performed another photolithography step, so I could lay metal in the trench. However, photoresist is supposed to be spun onto flat surfaces and the trench could cause the photoresist not to coat the entire surface of the wafer. After the metal deposition and lift-off, I could see that around the edges of the trench the photoresist had not covered the wafer and that metal had been deposited on those areas. Figure 61 shows the gold in

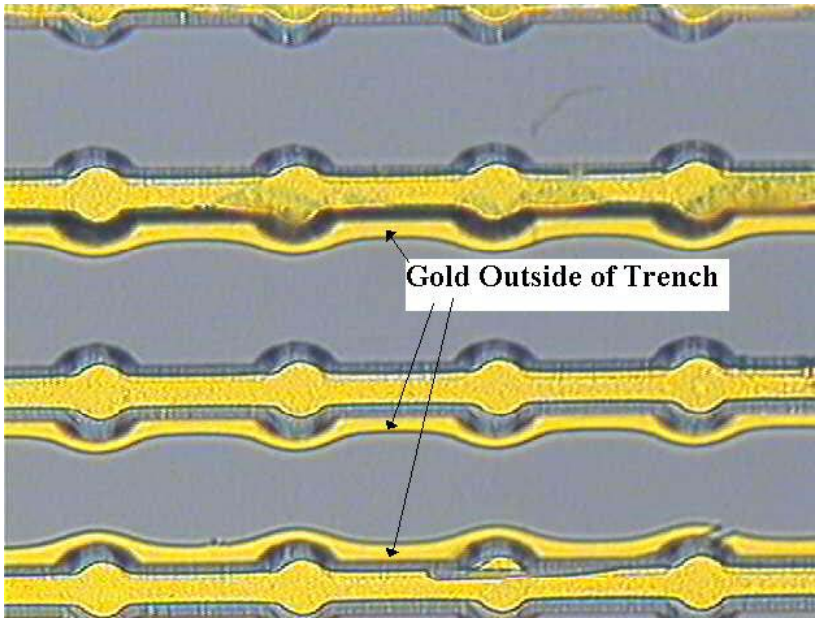

Figure 61 Microscope Image (20x) of bottom gold lines inside an 8 μm-deep trench. The trench the photoresist to spread unevenly over the wafer resulting in the gold depositing onto the sides of the trenches.

the trenches and on the edges. Though the metal was not confined to the trench, the gold on the sides of the trench should not affect the performance of the array and etching a trench is an easy way to achieve the small height difference requirement. One potential problem is that a gap would exist between the device and the trench. The gap is necessary for alignment tolerances, but would most likely result in the top metallization to fall down into the gap and create an open circuit. A photomask was designed (Section 3.9) to prevent this from happening. The idea is that photoresist could be spread onto the wafer and then developed out from everywhere except for the gap.

5.4.2 Build-Up Study. The next approach is to lay bottom metal down, then add an insulating material onto the wafer with a thickness equivalent to the height of the device, and finally deposit the top metal onto the insulating material. The material chosen for the studies was polymethylglutarimide (PMGI). PMGI is an insulating resist material that can be spun onto

a wafer in multi-layers and can also be patterned. The thickness of PMGI ranges from 50 nm to 8 μm for a single spun-on layer [1].

For this study, I first deposited metal on the wafer for the bottom layer of the array. Figures 62 and 63 show this metallization. Then, using MicroChem Corp Nano PMGI SF11, I was able to spin a 1.4 μm-thick coating onto the wafer (exact height of the device was not required, I simply wanted to validate the process). I then spun and patterned the 1813 photoresist and XPLOR 4A for the top metal layer deposition. I misaligned the mask on my first exposure and used the LDD26W to develop the photoresist, not knowing I had misaligned the mask. Upon inspection of the wafer, I noticed how poorly the alignment was done. I then removed the photoresist and XPLOR 4A to redo the alignment, but I noticed that the some of the PMGI was developed. I had concluded that the development of the PMGI was a result of overexposure. To correct for this, I reduced my exposure time from 6 seconds to 3 seconds. After my experiments, I was informed that the LDD26W used to develop the photoresist also develops the PMGI. The recess is shown in Figure 64.

After a better alignment, I laid down the gold, which is also shown in Figure 64. Slight problems occurred with the top metallization lift-off. Though the larger regions lifted-off cleanly, the narrow lines had a tendency of peeling off during development, suggesting that the photoresist was fully developed but not the underlying XPLOR4A, a consequence of changing the exposure times. Figure 65 shows the matrix array with the underlying metallization and the metallization deposited onto the PMGI. I again used the LDD26W in the development process, however, the recipe for the 1813 photoresist should be used (Appendix A) to avoid developing the PMGI. The final step, which was not performed in this study, would be to simply expose and develop the PMGI over the bottom metal contact pads so that they could be probed.

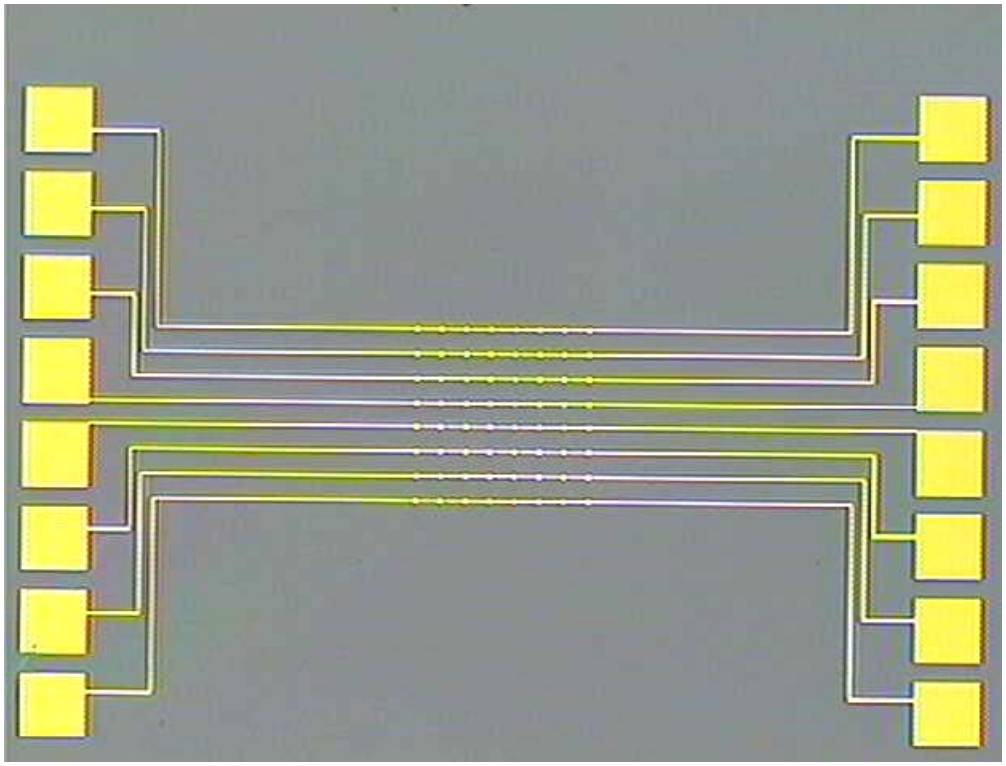

Figure 62 Microscope image (4x) of bottom metallization array.

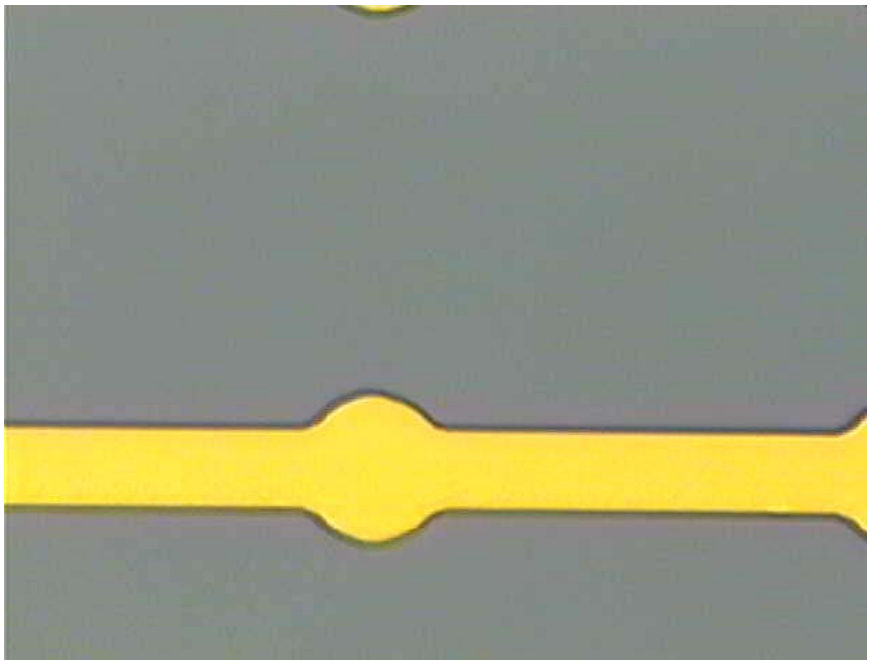

Figure 63 Microscope image (50x) of bottom metallization. Image focuses on one line and one circle. The circle is where the VCSEL would be placed.

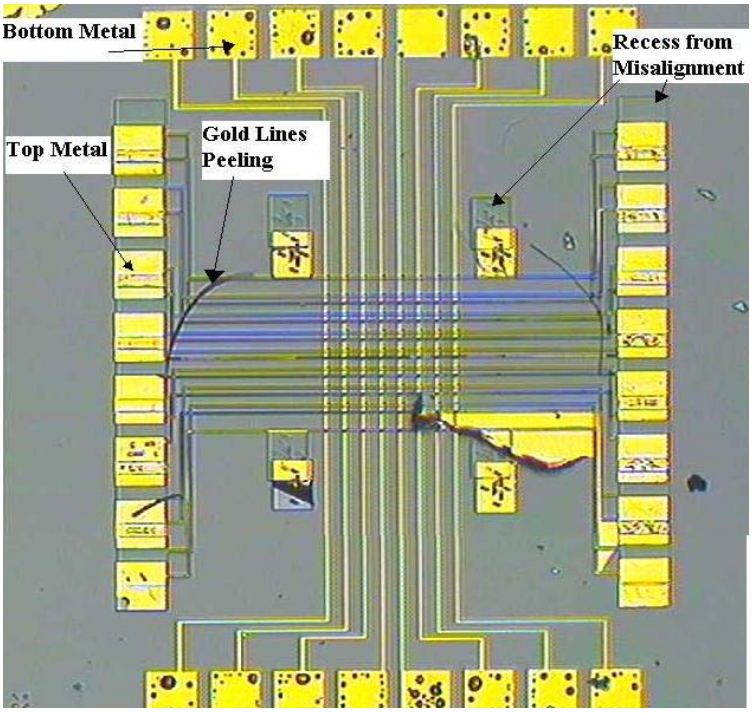

Figure 64 Microscope image (4x) of matrix array. The horizontal lines are running on top of the deposited PMGI layer. Some of the lines did not bond well to the PMGI and are peeling off.

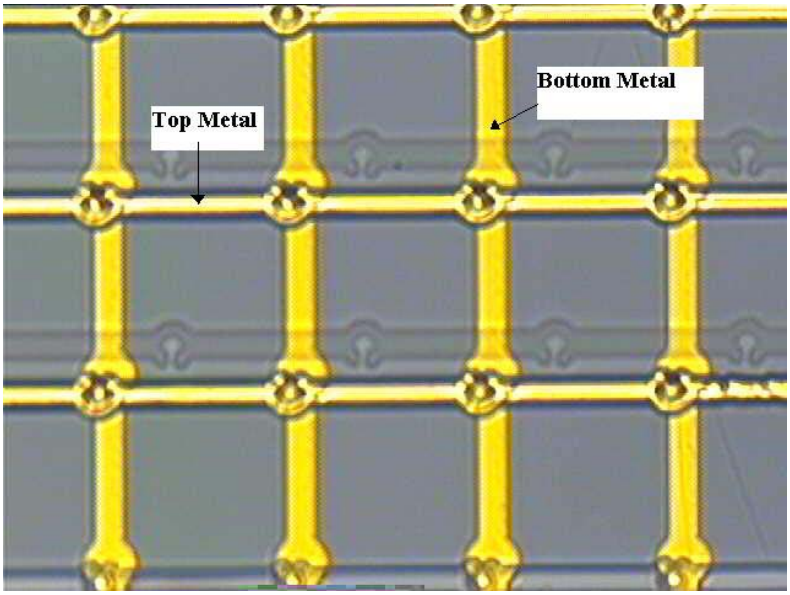

Figure 65 Microscope image (30x) illustrating the matrix array. The shadow shows the misalignment and subsequent recess of the PMGI. The top layer metallization is 1.4 μm higher than the bottom layer metallization.

5.4.3 Recess and Build-Up Study. The final study consisted of a combination of the first two approaches. The concept is to first etch a half trench, place the device in the trench, and then spin on PMGI level to the surface of the transplanted device. The possible advantages for this method include that multiple PMGI layers should not be required and the PMGI should be able to fill in the recess between the device and the edge of the recess.

A different approach was attempted for placing the metal in the trench. Rather than etching the trench and spinning on more photoresist, which was done in the first study, the photoresist used to etch the trench is also used during the deposition of the metal into the trench. By using this method, the problem with the unpredictable photoresist coverage is avoided. I etched two samples, one is 2 μm deep and the other is 3.5 μm deep. I then metallized and performed the metal lift-off. This time all the metal outside of the trench was successfully removed. Figures 66 and 67 show the result of the 3.5 μm etch and metallization. Figure 68 shows the 2 μm etch.

After metallization, I spun the PMGI onto the wafer to help reduce the height difference from the bottom metallization to the top metallization and to demonstrate the viability of this approach. I then spun the XPLOR 4A and 1805 photoresist onto the wafer and patterned it. Figure 69 shows the array with the bottom layer metallization and the patterning for the top layer metallization. As with the build-up approach, I again reduced my exposure times to prevent developing the PMGI. Because I reduced the exposure times, the photoresist was not fully developed for the smaller dimension structures causing the deposited metal to lift-off in those regions. The metal in the array remained on the wafer as shown in Figure 70, however, the metal lines running to the pads came off.

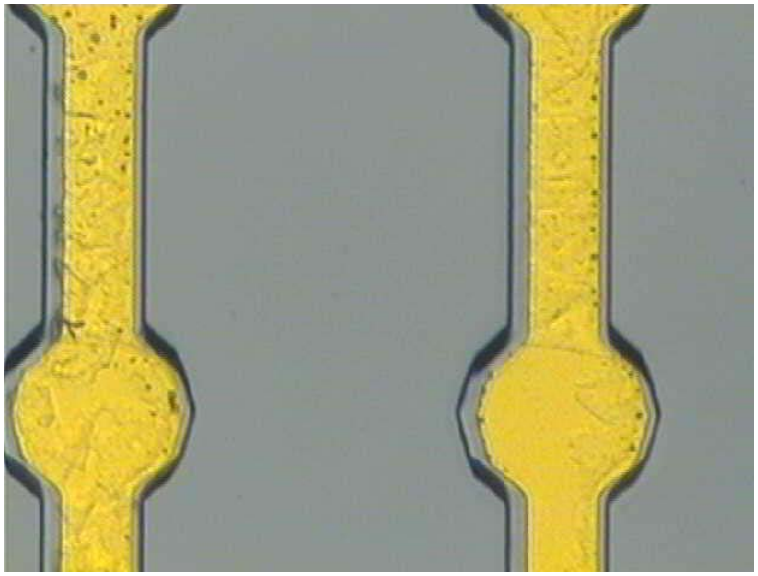

Figure 66 Microscope image (50x) of metallization in 3.5 μm trench

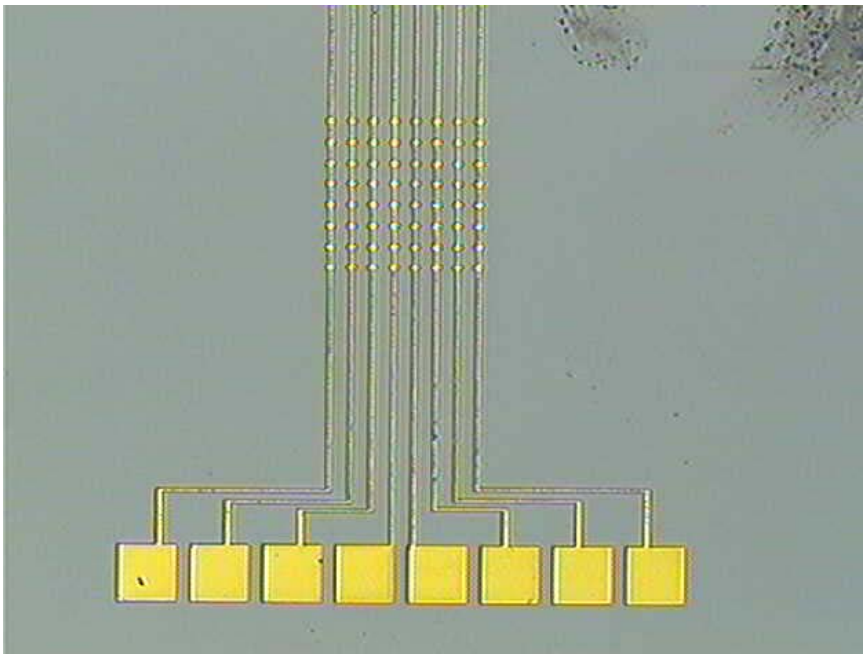

Figure 67 Microscope image (4x) of bottom metal in 3.5 μm trench.

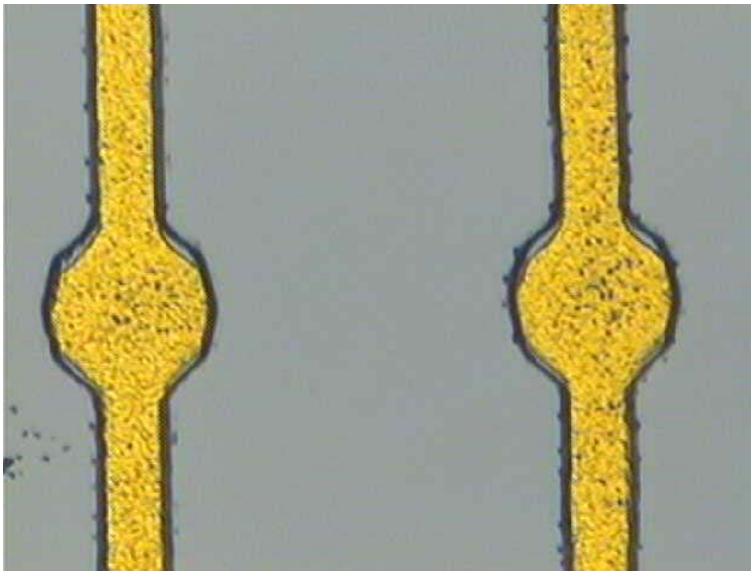

Figure 68 Microscope image (50x) of metal in 2 μm trench.

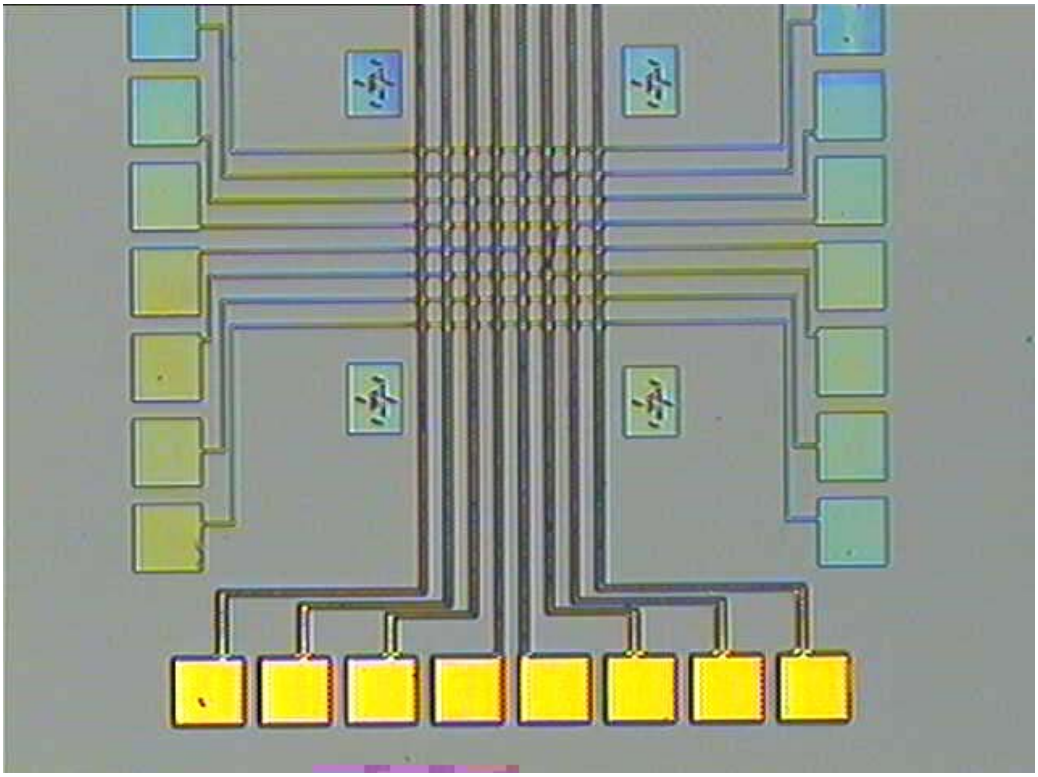

Figure 69 Microscope image (4x) of the patterned photoresist on top of the PMGI SF11.

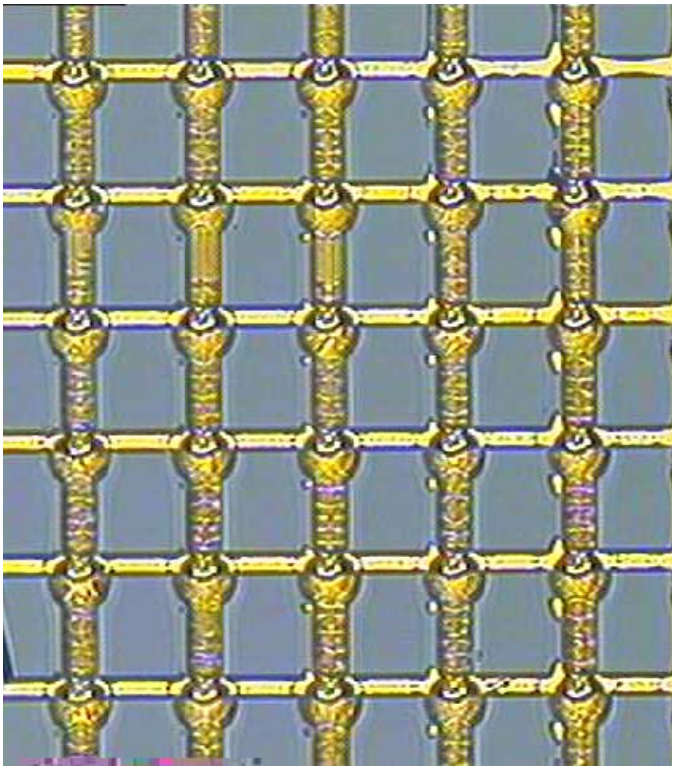

Figure 70 Microscope image (20x) of the bottom metallization and the top metallization running over them.

5.5 Summary

In this chapter, I presented the results of my MUMPs® array design. I also discussed the results of my VCSEL fabrication and unsuccessful wet etch to define mesas for the VCSEL. Finally, I presented the results of my studies on the fabrication of the matrix addressable array. I was able to demonstrate that metal could be placed into a recessed trench on the wafer, PMGI could then be spun onto the wafer, and another metallization layer could be patterned on top of the PMGI.

References

1. MicroChem website. http://www.microchem.com/products/pmgi_faq.htm. Taken on February 28, 2002.

6. Contributions, Lessons Learned, and Suggestions for Future Work

6.1 Contributions and Lessons Learned

I designed an array layout using the MUMPs® foundry process that can be used to fabricate a matrix-addressable array. I designed a set of photomasks that can be used to fabricate a matrix addressable array. The photomasks also contain designs for the processing and testing of micro-optical devices capable of integration with other substrates through either fluidic self-assembly or flip chip bonding techniques. I have demonstrated the viability of three approaches for the fabrication of a matrix addressable array.

I performed unsuccessful processes for the fabrication of micro-optical devices. I verified the notion that isotropic etches should not be used for 7.75 μm etches of 20 μm-diameter devices. For etches of this depth, device diameter should be at least 50 μm. An anisotropic etch is required for device fabrication with my mask set.

In my first approach for array fabrication, I etched a trench and deposited a gold layer in the trench. Experimenting with two different methods for depositing metal in the trench, I developed a process that places the metal in the trench and only in the trench. After the metal deposition, the micro-optical devices need to be transferred onto the metal and the top metal routing needs to be deposited.

In my second approach, I deposited metal onto the surface of the wafer. Next, I spun on a PMGI insulating layer. The top layer metallization is then deposited on top of the PMGI. In my experiments, I showed that the metal could be deposited onto the PMGI with marginal success. I discovered in my processing that the photolithographic process I used for metal deposition erodes the PMGI layer. The process follower in Appendix A should be used for this process

step. In this recipe, 351 developer is used and it will not erode the PMGI. Using this recipe, results for the metal deposition should be greatly improved.

In my final process, I use a combined approach. I demonstrated that metal could be deposited into the trench and the PMGI could then be spun-on. Again, the wrong recipe for the top metallization was used resulting in a poor top layer metallization.

I believe all three methods have advantages and disadvantages for fabricating the array. The first method is the simplest. In addition, placing the top metal directly onto the wafer is preferred over placing it onto the PMGI. However, the gap between the device and the edge of the hole presents a problem that must be addressed. The second method has the advantage that the gap problem should be eliminated, however, several PMGI layers might need to be spun on and developed to fabricate the array. The final approach is designed to reduce the disadvantages of each process. Hopefully, the PMGI layer will negate the gap problem and by using the trench only one PMGI layer is required. Additionally, the third approach is required to fabricate the matrix addressable micro-optical device arrays for the designs I created using the MUMPs® foundry process.

6.3 Future Work

My research has focused on fabrication techniques for lift-off microcavity device arrays. Further research is required on the integration of devices into the array. The easiest approach would be to flip-chip bond the devices onto the array, however, fluidic self-assembly approaches could also be a viable alternative that would eliminate the need for wafer alignment. Once the devices are in the array, the effects of the devices on the fabrication processes need to be studied. Processes to fill the gap or to create an air bridge between the device and the top of the trench should also be investigated for the deep trench array.

Additional approaches to fabricating arrays should also be attempted. One potential solution is to use layered metal routing similar to what designers do in very large-scale integrated circuits. By placing an insulating layer between levels of metal, the space required on the chip for routing will be reduced. Metal can be routed in between rows and columns of devices stacked on top of one another. This approach offers the potential to fabricate dense, large individually addressable micro-optical device arrays.

Appendix A: Photolithography Process Follower

Init.	Process Step	Notes
	Clean Wafer: ❑ 30 sec acetone rinse ❑ 30 sec methanol rinse ❑ 30 sec DI rinse ❑ Dry wafer with nitrogen	**Start Date**
	1813 Photoresist Coat: ❑ Flood wafer with 1813 photoresist ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑Use Acetone to remove resist on backside ❑ 75 sec 115 °C hot plate bake	**Start Time**
	EXPOSE 1813 with POST MASK: ❑ Align to wafer ❑ 15 sec exposure	
	1813 DEVELOP: ❑ 60 sec develop with 351:DI (1:5) ❑ 30 sec DI rinse ❑ Dry with nitrogen	
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition	

Appendix B: Metal Deposition Process Follower

MEM Tunable VCSEL – Ohmic Metal (Mask #1)		
12 February, 2002		Piece ID:
Init.	Process Step	Notes
	INSPECT WAFER: ❑ Note any defects	**Start Date** **Start Time**
	SOLVENT CLEAN: ❑ 20 sec acetone rinse at 500 rpm ❑ 20 sec isopropyl rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes	
	OXIDE REMOVAL: ❑ 30 sec dip (1:10) HCl:DI Water ❑ 3x DI Water bucket rinse ❑ Dry wafer with nitrogen on clean texwipes	
	DEHYDRATION BAKE: ❑ 1 min 110 °C Hot plate bake	
	XP LOR 3A Coat: ❑ Set spinner ramp rate = 200 ; spin 4000 rpm ❑ Coat sample with XP LOR 3A ❑ Spin 30 sec at 4,000 rpm, ramp=200 ❑ Use EBR to clean backside ❑ 2 minute HPB at 170° C ; cool	
	1805 COAT: ❑ Flood wafer with 1805 ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑ 75 sec 110°C hot plate bake ❑ Use acetone to remove 1813 on backside	
	Edge Bead Removal : ❑ Flood expose edge bead mask for 2 min (2mw/cm^2) ❑ Develop for 30 seconds using LDD26W developer ❑ DI rinse, N2 dry	
	EXPOSE 1805 with DC ELECTRODE MASK: ❑ Align to Bottom Metal alignment mark ❑ 17.5 sec Exposure	
	1805 DEVELOP: ❑ 75 sec develop with LDD26W at 1000 rpm ❑ 30 sec DI Water rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes ❑ Clean mask using acetone wipe and N_2 dry	
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition	
	ASHER DESCUM ❑ 4 min, 200 W, 400 sccm O_2, LFE Barrel Asher	
	PRE-METAL DIP: ❑ 30 sec Dip (1:7) BOE:DI Water ❑ 3x DI Water bucket rinse ❑ Dry wafer with nitrogen on clean texwipes	
	DC ELECTRODE METAL DEPOSITION: ❑ Evaporate 400 Å Ti / 2200Å Au (Titanium/Gold)	
	LIFT-OFF DC ELECTRODE METAL: ❑ 20 sec spray with acetone gun at 1000 rpm (pressurized @ 40 psi) ❑ 20 sec spray with acetone bottle at 500 rpm ❑ 30 sec spray with isopropyl alcohol at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes	

Process Step #1 **Revision 1.00** (15 Jan 02)

MEM Tunable VCSEL – Ohmic Metal (Mask #1)	
12 February, 2002	
	1165 STRIP XPLORE 3A: ❑ 5 min 90 °C 1165 remover ❑ 3x DI water bucket rinse ❑ Dry wafer with nitrogen on clean texwipes
	INSPECT WAFER: ❑ Inspect for resist removal under microscope **DEKTAK DC ELECTRODE HEIGHT:** ❑ Measure DC electrode step height using Dektak box Record height measurements:

Appendix C: PMGI Process Follower

Init.	Process Step	Notes
	DEHYDRATION BAKE: ❑ 1 min 110°C Hot plate bake	**Start Date**
	PMGI COAT #1: ❑ Flood wafer with SF-11 PMGI ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑ Use edge bead remover (EBR) to remove PMGI on backside (1 min @ 20°C) ❑ 1 min 270 °C hot plate bake	**Start Time**
	PMGI COAT #2 (USE FOR 2 µm BRIDGE HEIGHT): ❑ Flood wafer with SF-11 PMGI ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑ Use edge bead remover (EBR) to remove PMGI on backside (1 min @ 20°C) ❑ 1 min 270 °C hot plate bake	
	1813 COAT: ❑ Flood wafer with 1813 ❑ 30 sec spin at 4000 rpm, ramp=200 ❑ 75 sec 110 °C hot plate bake ❑ Use acetone to remove 1813 on backside	
	EXPOSE 1813 with POST MASK: ❑ Align to Bottom Metal alignment mark Right Key Offset **X** = 1.2700 Right Key Offset **Y** = 1.6075 ❑ 15.0 sec Exposure, 15 Focus on **Stepper**	**8520 \06**
	1813 DEVELOP: ❑ 60 sec develop with 351:DI (1:5) ❑ 30 sec DI rinse ❑ Dry with nitrogen ❑ Dry wafer with nitrogen on clean texwipes	
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition (Left) ❑ Measure vernier alignment on edge reticles in center row Theta (Right) X Alignment (Right) Y Alignment ❑ Rework wafer if alignment is off more than 0.6 µm	Y_{Left} = X_{Right} = Y_{Right} = $\theta = Y_{Right} - Y_{Left}$ =
	1ST DUV CYCLE (~1.5µm / cycle) ❑ 200 sec Deep UV exposure @ 35 mW/cm^2, 254 nm	
	PMGI DEVELOP: ❑ 60 sec SAL 101 spin develop at 500 rpm ❑ 30 sec DI water rinse at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes	
	INSPECT RESIST: ❑ Inspect photoresist	
	2ND DUV CYCLE ❑ 200 sec Deep UV exposure @ 35 mW/cm^2, 254 nm	
	PMGI DEVELOP ❑ 60 sec SAL 101 spin develop at 500 rpm ❑ 30 sec DI water rinse at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes	
	INSPECT RESIST: ❑ Inspect photresist	

	STRIP 1813: ❑ 20 sec acetone gun at 1000 rpm ❑ 20 sec acetone rinse at 500 rpm ❑ 30 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes	
	INSPECT RESIST: ❑ Inspect photoresist for 1813 removal	
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE	
	DEKTAK POST HEIGHT: ❑ Measure resist step height in three locations Top _____ Middle _____ Bottom _____	
	POST REFLOW & INSPECT WAFER: ❑ 120 sec 250 °C hot air oven bake **USE OVEN TRAY** Start timer after door is closed ❑ Inspect for resist reflow. Reflow again if necessary	**Reflow Time:**
	TENCOR MEASURE: ❑ Measure resist step height in center and save Tencor profile. Resist Height: _____	**Finish Date**
	HARD BAKE: ❑ Place in 90 °C hot air oven 60 min before bridge lithography	**Finish Time**

Vita

Ryan Daniel Conk was commissioned into the United States Air Force after successful completion of his undergraduate studies at the University of California, Los Angeles where he received a B. S. in Electrical Engineering in June of 2000. He was selected as a direct accession to the Air Force Institute of Technology at Wright-Patterson AFB, OH where he received his M.S. in Electrical Engineering. Lt Conk's next assignment will be at the National Air Intelligence Center at Wright-Patterson Air Force Base.

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14. ABSTRACT Micro-optical devices are vital components of conventional military data storage, sensor, and communication systems. The matrix addressable array has a drastically reduced number of metal lines and can potentially be fabricated into large, dense (over 1k elements) arrays. Such arrays are expected to enable the development of extremely high bandwidth optical interconnect systems for future military applications including optical computing and short-haul fiber optical communication systems.
I investigate new fabrication techniques for the assembly of dense matrix-addressed arrays of micro-optical devices such as vertical-cavity surface-emitting lasers. Using a micro-electro-mechanical systems (MEMS) foundry process, I design a test chip that consists of a variety of array configurations to explore possible assembly techniques. I also design a new photolithographic mask set based on assembly by flip-chip bonding and fluidic self-assembly techniques. Using my mask set, I perform basic fabrication studies and an analysis of metallization schemes for the realization of dense emitter and detector arrays. Finally, I develop and characterize three methods for array fabrication including a novel substrate trenching technique and involving the use of a spin-on polymer (poly-methyl-glutarimide or PMGI) that serves as an insulating and planarization layer between row and column metal lines.

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